FAIRCHILD SEMICONDUCTOR™

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MM74C157
Quad 2-Input Multiplexers

General Description

The MM74C157 multiplexers are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement transistors. They consist of four 2-input multiplexers with common select and enable inputs. When the enable input is at logical "0" the four outputs assume the values as selected from the inputs. When the enable input is at logical "1", the outputs assume logical "0". Select decoding is done internally resulting in a single select input only.

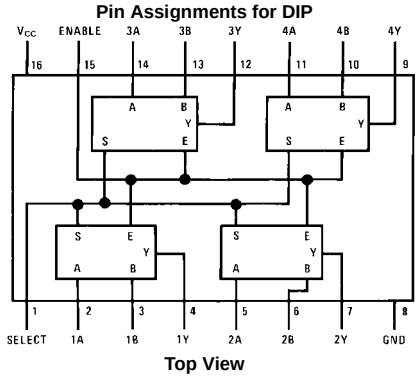
Features

- Supply voltage range: 3V to 15V
- High noise immunity: 0.45 V_{CC} (typ.)
- Low power: 50 nW (typ.)
- Tenth power TTL compatible: Drive 2 LPTTL loads

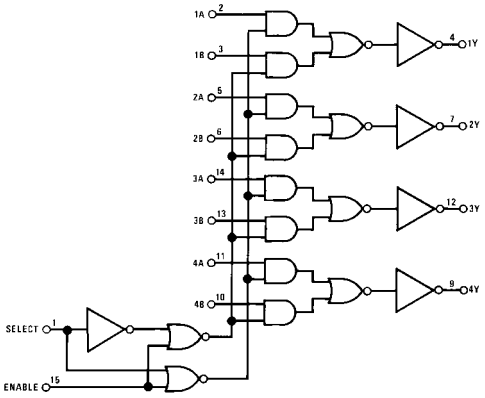
Ordering Code:

Order Number	Package Number	Package Description
MM74C157N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram



Logic Diagram



Truth Table

Enable	Select	A	B	Output Y
1	X	X	X	0
0	0	0	X	0
0	0	1	X	1
0	1	X	0	0
0	1	X	1	1

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum V_{CC} Voltage	18V
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Lead Temperature (Soldering, 10 seconds)	260°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	3.5			V
		V_{CC} = 10V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			1.5	V
		V_{CC} = 10V			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V	4.5			V
		V_{CC} = 10V	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V			0.5	V
		V_{CC} = 10V			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V		0.005	1.0	µA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V	−1.0	−0.005		µA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	60	µA
CMOS TO TENTH POWER INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 4.75V	V_{CC} − 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75V, I_O = −360 µA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 4.75V, I_O = 360 µA			0.4	V
OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	V_{CC} = 5V, $V_{IN(0)}$ = 0V	−1.75			mA
		T_A = 25°C, V_{OUT} = 0V				
I_{SOURCE}	Output Source Current	V_{CC} = 10V, $V_{IN(0)}$ = 0V	−8.0			mA
		T_A = 25°C, V_{OUT} = 0V				
I_{SINK}	Output Sink Current	V_{CC} = 5V, $V_{IN(1)}$ = 5V	1.75			mA
		T_A = 25°C, V_{OUT} = V_{CC}				
I_{SINK}	Output Sink Current	V_{CC} = 10V, $V_{IN(1)}$ = 10V	8.0			mA
		T_A = 25°C, V_{OUT} = V_{CC}				

AC Electrical Characteristics (Note 2)

$T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay from	$V_{CC} = 5.0V$		150	250	ns
	Data to Output	$V_{CC} = 10V$		70	110	ns
t_{pd0}, t_{pd1}	Propagation Delay from	$V_{CC} = 5V$		180	300	ns
	Select to Output	$V_{CC} = 10V$		80	130	ns
t_{pd0}, t_{pd1}	Propagation Delay from	$V_{CC} = 5V$		180	300	ns
	Enable to Output	$V_{CC} = 10V$		80	130	ns
C_{IN}	Input Capacitance	(Note 3)		5		pF
C_{PD}	Power Dissipation	(Note 4)		20		pF
	Capacitance					

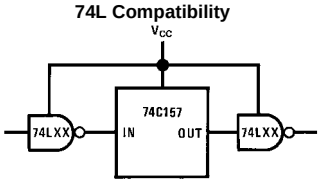
Note 2: AC Parameters are guaranteed by DC correlated testing.

Note 3: Capacitance is guaranteed by periodic testing.

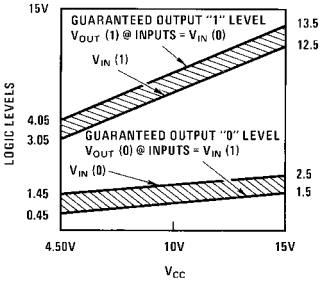
Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see Family Characteristics, Application Note AN-90.

Typical Applications

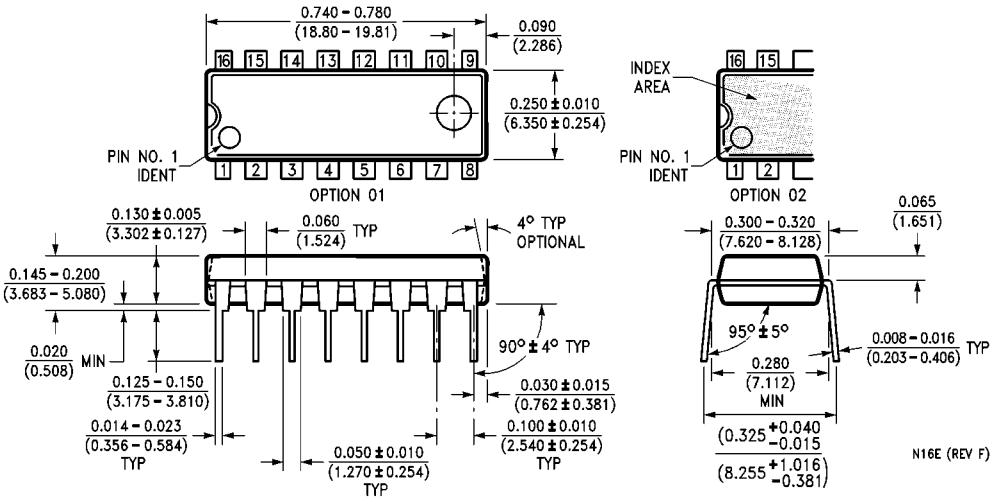
74L Compatibility



Guaranteed Noise Margin as a Function of V_{CC}



Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001. 0.300" Wide
Package Number N16E

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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