Na t i o n a l *S e m i c o n d u c t o r*

MM54C914/MM74C914 Hex Schmitt Trigger with Extended Input Voltage

General Description

The MM54C914/MM74C914 is a monolithic CMOS Hex Schmitt trigger with special input protection scheme. This scheme allows the input voltage levels to exceed V_{CC} or ground by at least 10V ($V_{CC} - 25V$ to GND + 25V), and is valuable for applications involving voltage level shifting or mismatched power supplies.

The positive and negative-going threshold voltages, V_{T+} and V_{T-}, show low variation with respect to temperature (typ 0.0005V/°C at $V_{CC} = 10V$). And the hysteresis, $V_{T+} - V_{T-} \geq 0.2 V_{CC}$ is guaranteed.
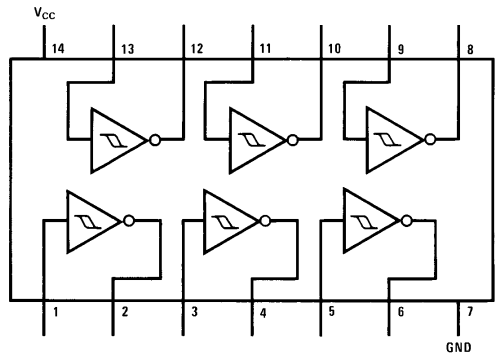
Features

■ Hysteresis   0.45 V_{CC} (typ.)
                            0.2 V_{CC} guaranteed
■ Special input protection   Extended Input
                               Voltage Range
■ Wide supply voltage range   3V to 15V
■ High noise immunity   0.7 V_{CC} (typ.)
■ Low power TTL   Fan out of 2
  compatibility   driving 74L

Connection Diagram

Dual-In-Line Package

TL/F/5917–1

Top View

Order Number MM54C914 or MM74C914

Special Input Protection

8V ≈ 25V
for the diodes.

TL/F/5917–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at any Input Pin	$V_{CC} - 25V$ to GND $+ 25V$
Voltage at any other Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range (T_A)	
MM54C914	$-55°C$ to $+125°C$
MM74C914	$-40°C$ to $+85°C$

Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum (V_{CC})	18V
Lead Temperature (T_L)	
(Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
V_{T+}	Positive Going Threshold Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$	3.0 6.0 9.0	3.6 6.8 10	4.3 8.6 12.9	V V
V_{T-}	Negative Going Threshold Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$	0.7 1.4 2.1	1.4 3.2 5	2.0 4.0 6.0	V V
$V_{T+} - V_{T-}$	Hysteresis	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$	1.0 2.0 3.0	2.2 3.6 5	3.6 7.2 10.8	V V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V$, $I_O = -10 \mu A$ $V_{CC} = 10V$, $I_O = -10 \mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V$, $I_O = +10 \mu A$ $V_{CC} = 10V$, $I_O = +10 \mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 25V$		0.005	5.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = -10V$	-100	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$, $V_{IN} = -10V/25V$ $V_{CC} = 5V$, $V_{IN} = -2.5V$ (Note 4) $V_{CC} = 10V$, $V_{IN} = 5V$ (Note 4) $V_{CC} = 15V$, $V_{IN} = 7.5V$ (Note 4)		0.05 20 200 600	300	μA μA μA μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	4.3			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$			0.7	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = -360 \mu A$ 74C, $V_{CC} = 4.75V$, $I_O = -360 \mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = 360 \mu A$ 74C, $V_{CC} = 4.75V$, $I_O = 360 \mu A$			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5V$, $V_{OUT} = 0V$, $T_A = 25°C$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$, $T_A = 25°C$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5V$, $V_{OUT} = V_{CC}$, $T_A = 25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V$, $V_{OUT} = V_{CC}$, $T_A = 25°C$	8.0	16		mA

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay from Input to Output	$V_{CC} = 5V$		220	400	ns
		$V_{CC} = 10V$		80	200	ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		20		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

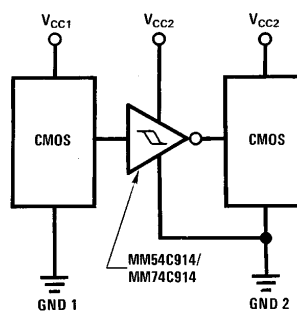**Note 2:** Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note, AN-90.

Note 4: Only one input is at ½ V_{CC}, the others are either at V_{CC} or GND.
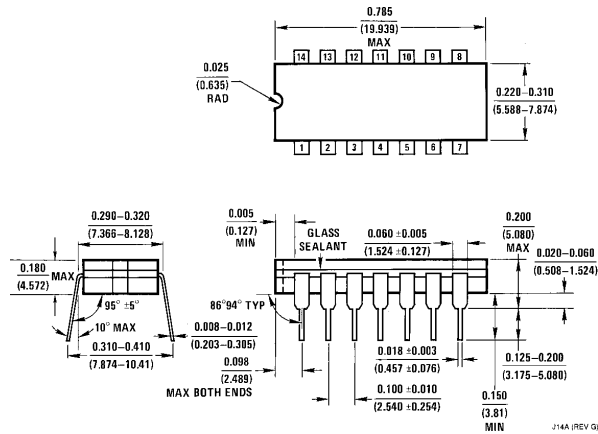
Typical Performance Characteristics

Typical Transfer Characteristics

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Guaranteed Trip Point Range

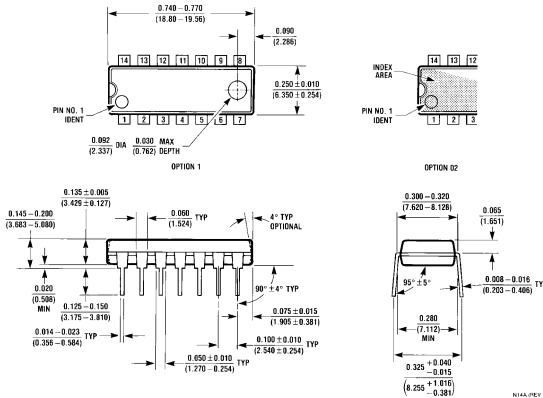TL/F/5917–5

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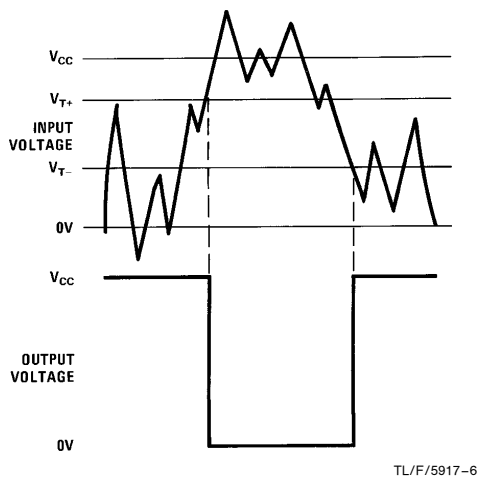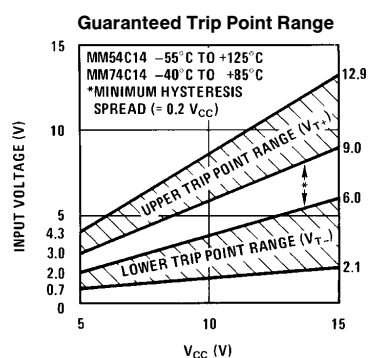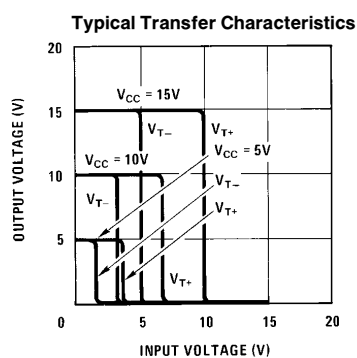
Typical Application

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Note: $V_{CC1} = V_{CC2}$
GND1 = GND2

Physical Dimensions inches (millimeters)

Ceramic Dual-In-Line Package (J)
Order Number MM54C914J or MM74C914J
NS Package Number J14A

Molded Dual-In-Line Package (N)
Order Number MM54C914N or MM74C914N
NS Package Number N14A

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