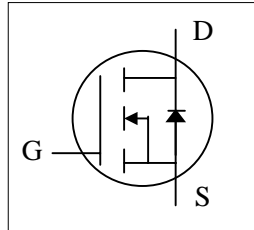




- ▼ Simple Drive Requirement
- ▼ Lower On-resistance
- ▼ High Speed Switching

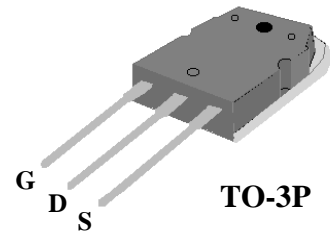


BV_{DSS}	300V
$R_{DS(ON)}$	48m Ω
I_D	48A

Description

AP88N30 from APEC provide the designer with the best combination of fast switching, low on-resistance and cost-effectiveness.

The TO-3P package is preferred for commercial & industrial applications with higher power level preclusion than TO-220 device.



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	300	V
V_{GS}	Gate-Source Voltage	+30	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	48	A
I_{DM}	Pulsed Drain Current ¹	160	A
I_{DR}	Body-Drain Diode Reverse Drain Current	48	A
$I_{DR(PULSE)}$	Body-Drain Diode Reverse Drain Peak Current ¹	160	A
$P_D@T_C=25^\circ C$	Total Power Dissipation	312	W
	Linear Derating Factor	1.2	W/ $^\circ C$
I_{AR}	Avalanche Current	30	A
E_{AR}	Single Pulse Avalanche Energy ³	45	mJ
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	0.4	$^\circ C/W$
Rthj-a	Maximum Thermal Resistance, Junction-ambient	40	$^\circ C/W$



AP88N30W

Electrical Characteristics @T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	300	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =30A	-	-	48	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	3	-	4.5	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =30A	-	62	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =300V, V _{GS} =0V	-	-	1	uA
	Drain-Source Leakage Current (T _j =125°C)	V _{DS} =240V, V _{GS} =0V	-	-	200	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±30V, V _{DS} =0V	-	-	±0.1	uA
Q _g	Total Gate Charge ²	I _D =30A	-	150	250	nC
Q _{gs}	Gate-Source Charge	V _{DS} =240V	-	35	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =10V	-	60	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =150V	-	50	-	ns
t _r	Rise Time	I _D =30A	-	105	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =10Ω	-	220	-	ns
t _f	Fall Time	V _{GS} =10V	-	110	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	8440	13500	pF
C _{oss}	Output Capacitance	V _{DS} =15V	-	1775	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	70	-	pF
R _g	Gate Resistance	f=1.0MHz	-	2.2	3.3	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =30A, V _{GS} =0V	-	-	1.5	V
t _{rr}	Reverse Recovery Time ²	I _S =10A, V _{GS} =0V	-	300	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	3.8	-	μC

Notes:

- 1.Pulse width limited by max. junction temperature
- 2.Pulse test
- 3.Starting T_j=25°C , V_{DD}=50V , L=1mH , R_G=25Ω , I_{AS}=30A.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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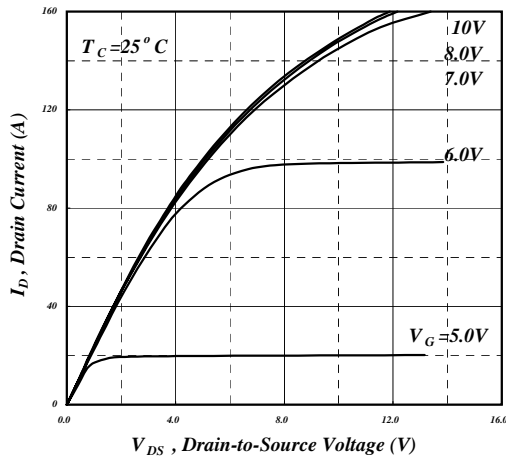


Fig 1. Typical Output Characteristics

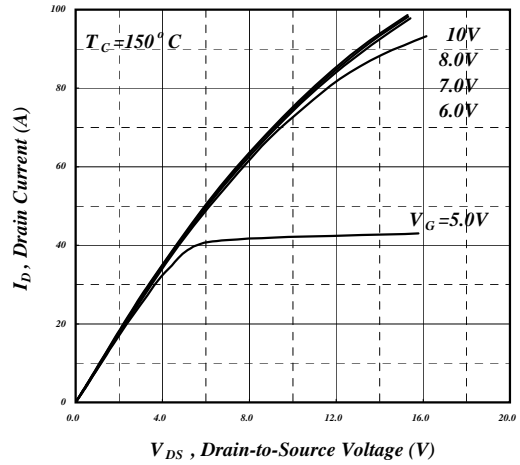


Fig 2. Typical Output Characteristics

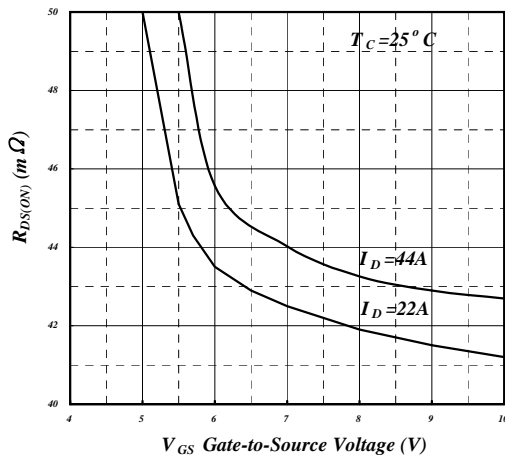


Fig 3. On-Resistance v.s. Gate Voltage

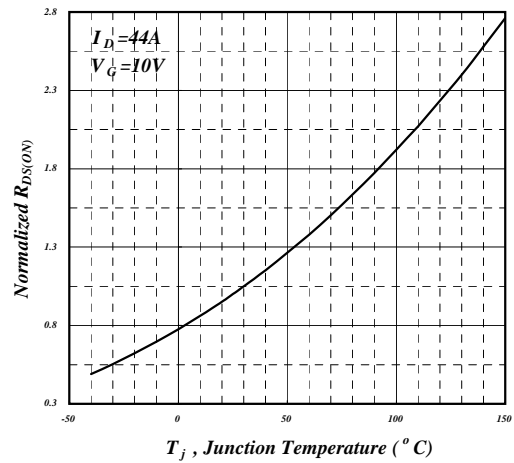


Fig 4. Normalized On-Resistance v.s. Junction Temperature

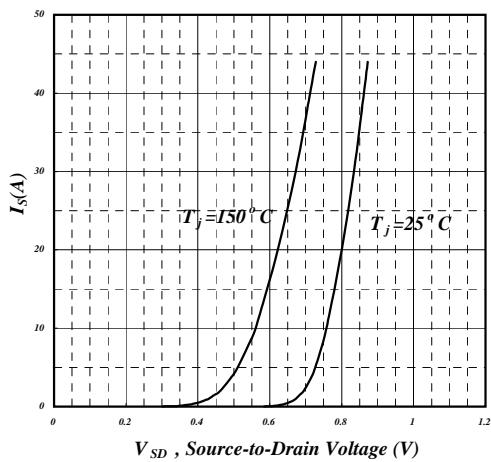


Fig 5. Forward Characteristic of Reverse Diode

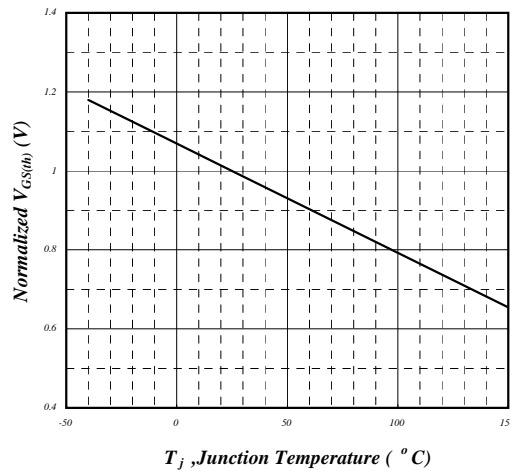


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

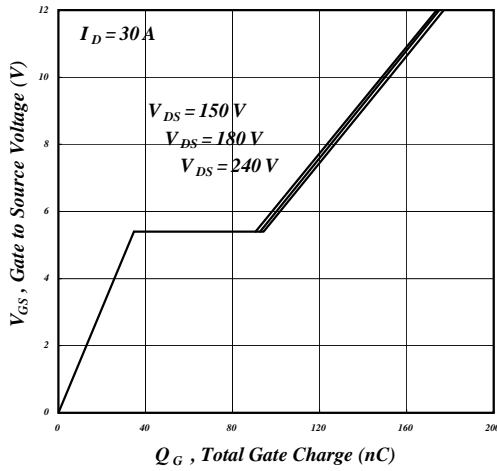


Fig 7. Gate Charge Characteristics

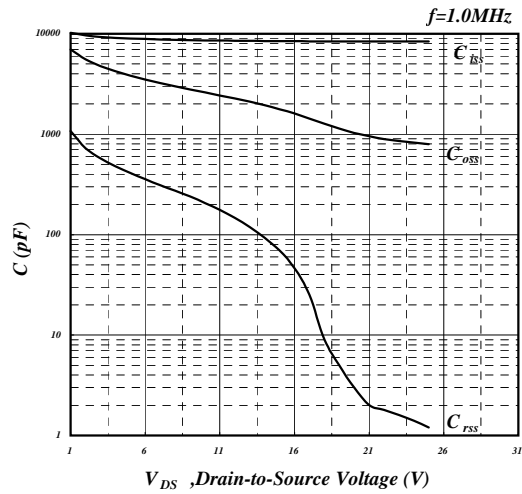


Fig 8. Typical Capacitance Characteristics

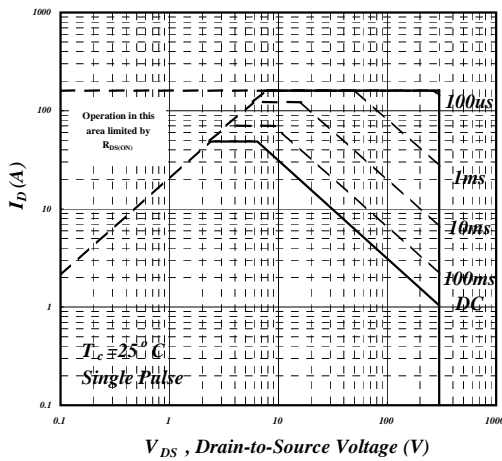


Fig 9. Maximum Safe Operating Area

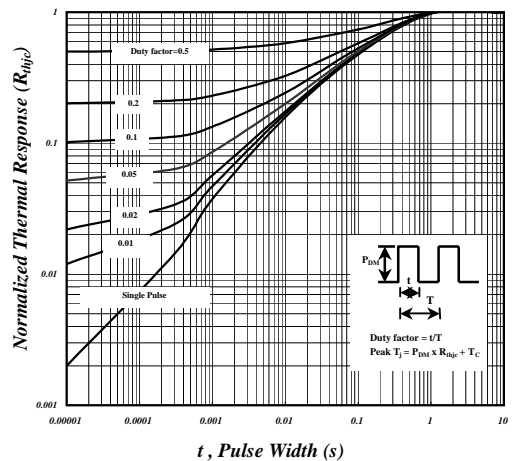


Fig 10. Effective Transient Thermal Impedance

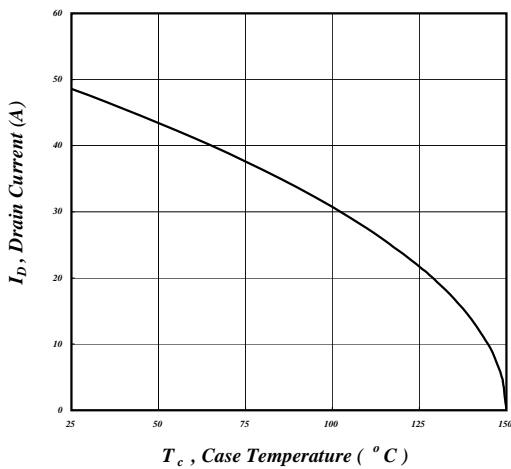


Fig 11. Maximum Drain Current v.s. Case Temperature

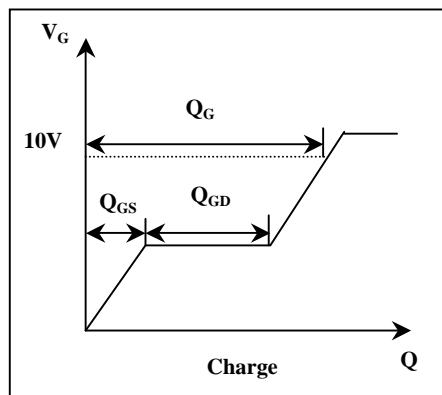


Fig 12. Gate Charge Waveform