

Dual Enhancement Mode MOSFET (N- and P-Channel)

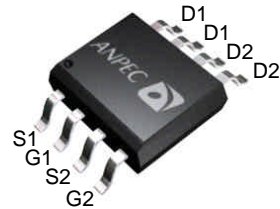
Features

- N-Channel
40V/6.5A,
 $R_{DS(ON)} = 20m\Omega$ (typ.) @ $V_{GS} = 10V$
 $R_{DS(ON)} = 28m\Omega$ (typ.) @ $V_{GS} = 4.5V$
- P-Channel
-40V/-5A,
 $R_{DS(ON)} = 35m\Omega$ (typ.) @ $V_{GS} = -10V$
 $R_{DS(ON)} = 48m\Omega$ (typ.) @ $V_{GS} = -4.5V$
- Super High Dense Cell Design
- Reliable and Rugged
- Lead Free and Green Devices Available
(RoHS Compliant)

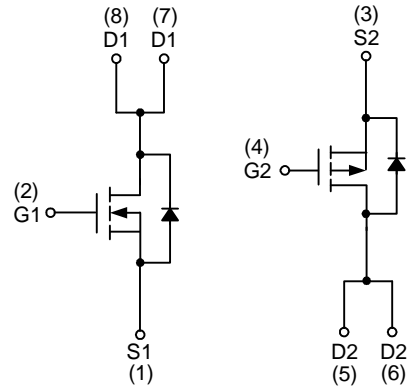
Applications

- Power Management in Notebook Computer,
Portable Equipment and Battery Powered
Systems

Pin Description



Top View of SOP – 8



N-Channel MOSFET P-Channel MOSFET

Ordering and Marking Information

<p>APM4568 □□-□□ □</p> <div style="margin-left: 20px;"> <p>└─ Assembly Material</p> <p>└─ Handling Code</p> <p>└─ Temperature Range</p> <p>└─ Package Code</p> </div>	<p>Package Code K : SOP-8</p> <p>Operating Junction Temperature Range C : -55 to 150 °C</p> <p>Handling Code TR : Tape & Reel</p> <p>Assembly Material G : Halogen and Lead Free Device</p>
<p>APM4568 K :</p> <div style="border: 1px solid black; padding: 2px; display: inline-block; margin-left: 10px;"> <p>APM4568 XXXXX ●</p> </div>	<p>XXXXX - Date Code</p>

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Absolute Maximum Ratings $(T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating		Unit	
		N Channel	P Channel		
V_{DSS}	Drain-Source Voltage	40	-40	V	
V_{GSS}	Gate-Source Voltage	± 20	± 20		
I_D^*	Continuous Drain Current	$V_{GS}=10\text{V (N)}$	6.5	-5	A
I_{DM}^*	Pulsed Drain Current	$V_{GS}=-10\text{V (P)}$	25	-20	
I_S^*	Diode Continuous Forward Current		2.5	-2.5	A
T_J	Maximum Junction Temperature	150		$^\circ\text{C}$	
T_{STG}	Storage Temperature Range	-55 to 150			
P_D^*	Power Dissipation	$T_A=25^\circ\text{C}$	2		W
		$T_A=100^\circ\text{C}$	0.8		
$R_{\theta JA}^*$	Thermal Resistance-Junction to Ambient	62.5		$^\circ\text{C/W}$	

Note : *Surface Mounted on 1in^2 pad area, $t \leq 10\text{sec}$.

Electrical Characteristics $(T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	APM4568K			Unit	
			Min.	Typ.	Max.		
Static Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_{DS}=250\mu\text{A}$	N-Ch	40	-	-	V
		$V_{GS}=0\text{V}, I_{DS}=-250\mu\text{A}$	P-Ch	-40	-	-	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=32\text{V}, V_{GS}=0\text{V}$ $T_J=85^\circ\text{C}$	N-Ch	-	-	1	μA
			P-Ch	-	-	-1	
		$V_{DS}=-32\text{V}, V_{GS}=0\text{V}$ $T_J=85^\circ\text{C}$	N-Ch	-	-	30	
			P-Ch	-	-	-30	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=250\mu\text{A}$	N-Ch	1.3	2	2.5	V
		$V_{DS}=V_{GS}, I_{DS}=-250\mu\text{A}$	P-Ch	-1.3	-1.9	-2.5	
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$	N-Ch	-	-	± 100	nA
		$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$	P-Ch	-	-	± 100	
$R_{DS(ON)a}$	Drain-Source On-State Resistance	$V_{GS}=10\text{V}, I_{DS}=6.5\text{A}$	N-Ch	-	20	28	m Ω
		$V_{GS}=-10\text{V}, I_{DS}=-5\text{A}$	P-Ch	-	35	48	
		$V_{GS}=4.5\text{V}, I_{DS}=4.5\text{A}$	N-Ch	-	28	42	
		$V_{GS}=-4.5\text{V}, I_{DS}=-3\text{A}$	P-Ch	-	48	68	

Electrical Characteristics (Cont.) ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	APM4568K			Unit	
			Min.	Typ.	Max.		
Diode Characteristics							
V_{SD}^a	Diode Forward Voltage	$I_{SD}=2A, V_{GS}=0V$	N-Ch	-	0.8	1.1	V
		$I_{SD}=-2A, V_{GS}=0V$	P-Ch	-	-0.8	-1.1	
Dynamic Characteristics^b							
R_G	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, F=1\text{MHz}$	N-Ch	-	2	-	Ω
			P-Ch	-	8	-	
C_{iss}	Input Capacitance	N-Channel $V_{GS}=0V,$ $V_{DS}=20V,$ Frequency=1.0MHz	N-Ch	-	980	-	pF
C_{oss}	Output Capacitance		P-Ch	-	1095	-	
C_{rss}	Reverse Transfer Capacitance	P-Channel $V_{GS}=0V,$ $V_{DS}=-20V,$ Frequency=1.0MHz	N-Ch	-	110	-	
			P-Ch	-	125	-	
$t_{d(ON)}$	Turn-on Delay Time	N-Channel $V_{DD}=20V, R_L=20\Omega,$ $I_{DS}=1A, V_{GEN}=10V,$ $R_G=6\Omega$	N-Ch	-	16	30	ns
			P-Ch	-	12	23	
T_r	Turn-on Rise Time	P-Channel $V_{DD}=-20V, R_L=20\Omega,$ $I_{DS}=-1A, V_{GEN}=-10V,$ $R_G=6\Omega$	N-Ch	-	19	35	
			P-Ch	-	21	39	
$t_{d(OFF)}$	Turn-off Delay Time	N-Channel $V_{DD}=20V, R_L=20\Omega,$ $I_{DS}=1A, V_{GEN}=10V,$ $R_G=6\Omega$	N-Ch	-	30	55	
			P-Ch	-	43	78	
T_f	Turn-off Fall Time	P-Channel $V_{DD}=-20V, R_L=20\Omega,$ $I_{DS}=-1A, V_{GEN}=-10V,$ $R_G=6\Omega$	N-Ch	-	6	12	
t_{rr}	Reverse Recovery Time	N-Channel $I_{SD}=6.5A, dI_{SD}/dt = 100A/\mu s$	N-Ch	-	20	-	ns
			P-Ch	-	19	-	
Q_{rr}	Reverse Recovery Charge	P-Channel $I_{SD}=-5A, dI_{SD}/dt = 100A/\mu s$	N-Ch	-	14	-	nC
			P-Ch	-	12	-	
Gate Charge Characteristics^b							
Q_g	Total Gate Charge	N-Channel $V_{DS}=20V, V_{GS}=10V,$ $I_{DS}=6.5A$	N-Ch	-	20	28	nC
			P-Ch	-	20	28	
Q_{gs}	Gate-Source Charge	P-Channel $V_{DS}=-20V, V_{GS}=-10V,$ $I_{DS}=-5A$	N-Ch	-	3	-	
			P-Ch	-	3.5	-	
Q_{gd}	Gate-Drain Charge	N-Channel $V_{DS}=20V, V_{GS}=10V,$ $I_{DS}=6.5A$	N-Ch	-	6	-	
			P-Ch	-	3.5	-	

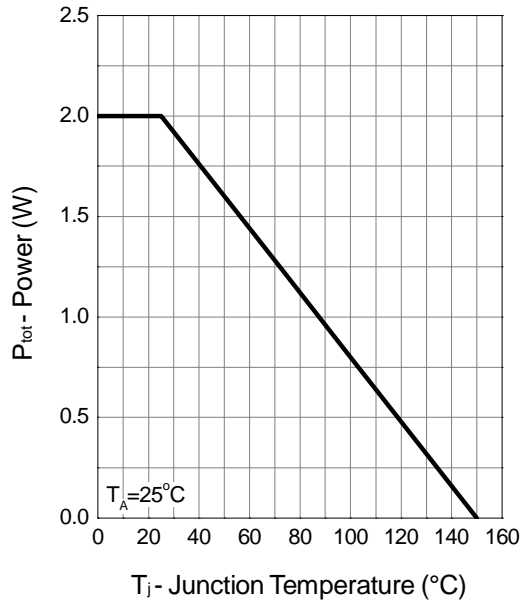
Note a : Pulse test ; pulse width \leq 300ms, duty cycle \leq 2%.

Note b : Guaranteed by design, not subject to production testing.

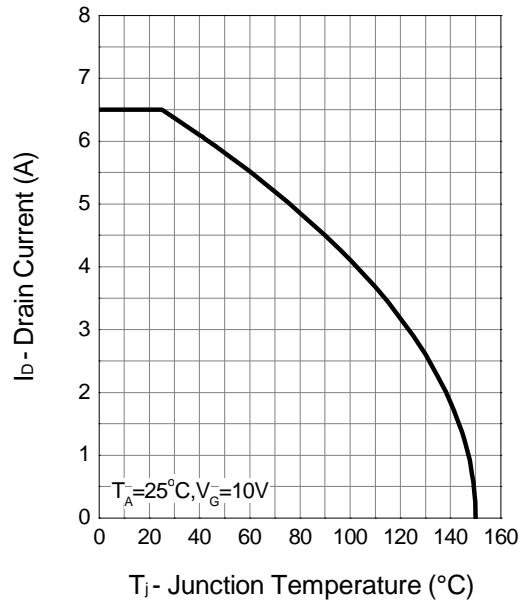
Typical Operating Characteristics

N-Channel

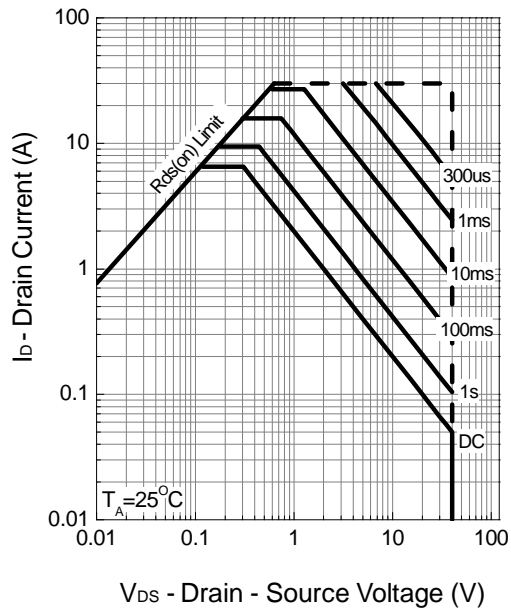
Power Dissipation



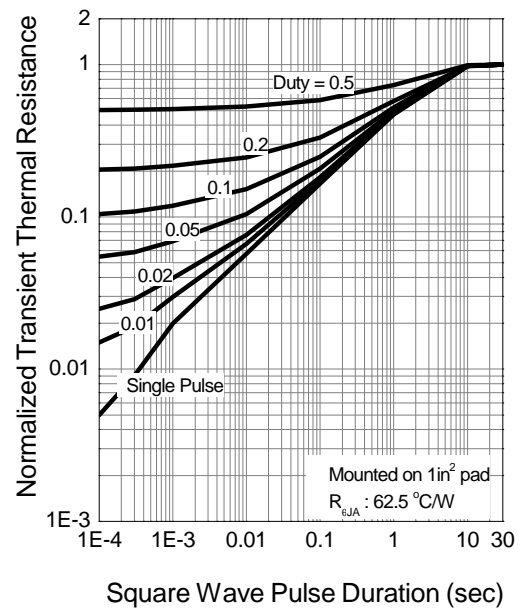
Drain Current



Safe Operation Area



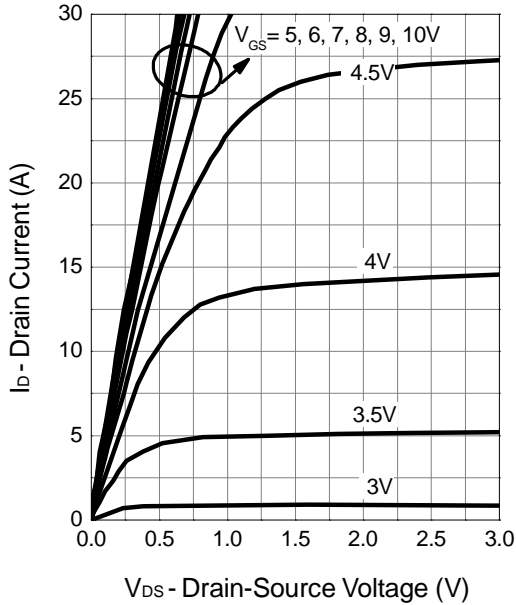
Thermal Transient Impedance



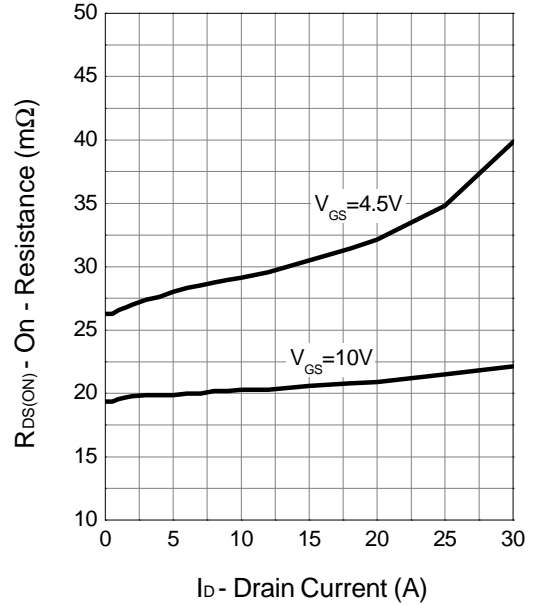
Typical Operating Characteristics (Cont.)

N-Channel

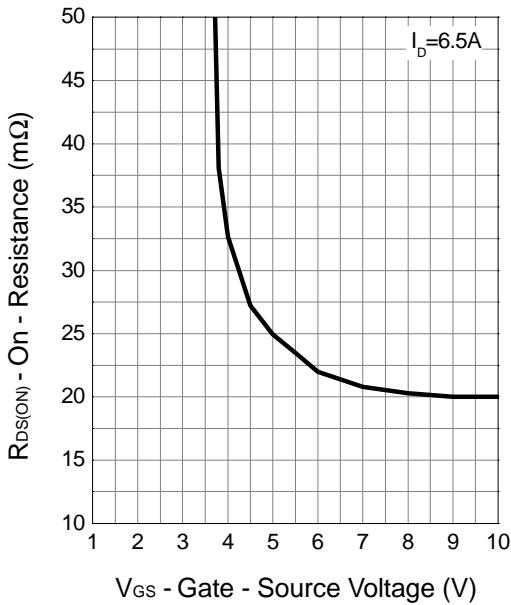
Output Characteristics



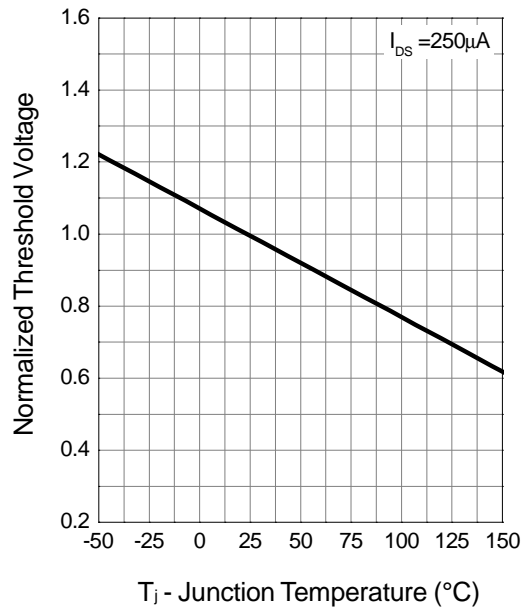
Drain-Source On Resistance



Drain-Source On Resistance



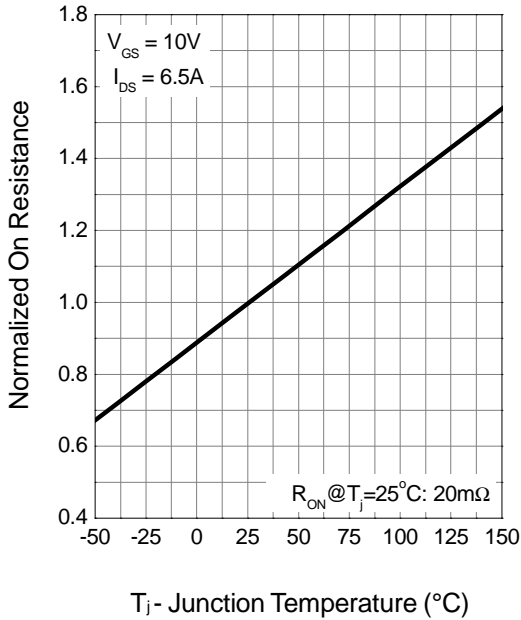
Gate Threshold Voltage



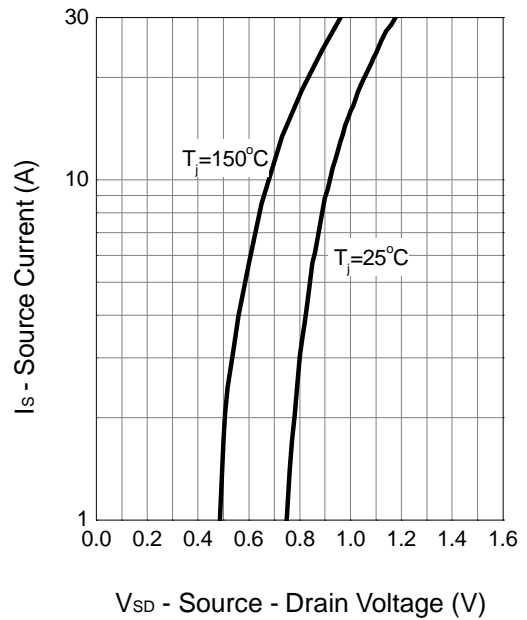
Typical Operating Characteristics (Cont.)

N-Channel

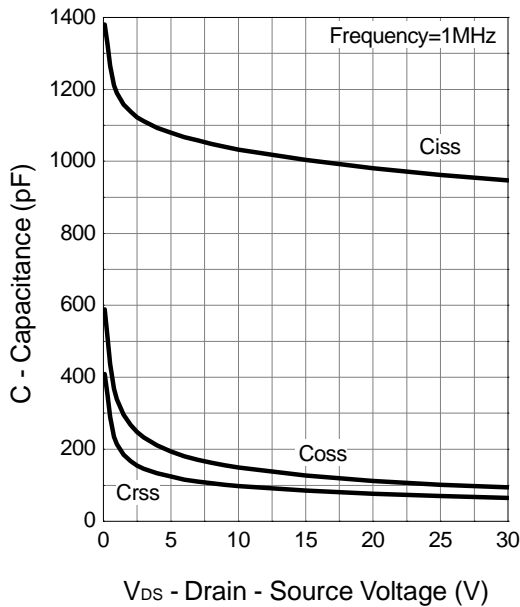
Drain-Source On Resistance



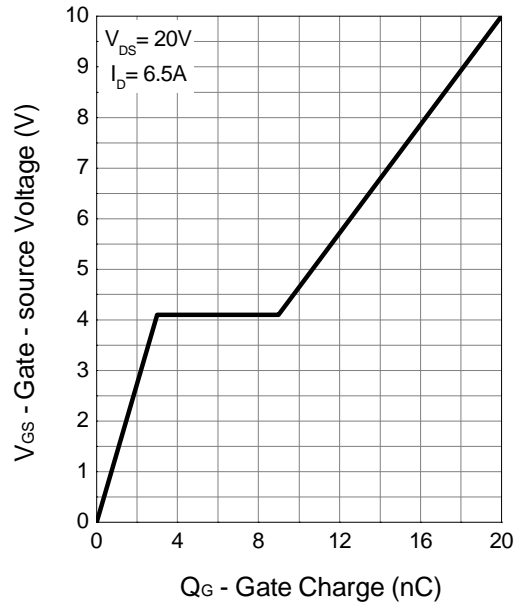
Source-Drain Diode Forward



Capacitance



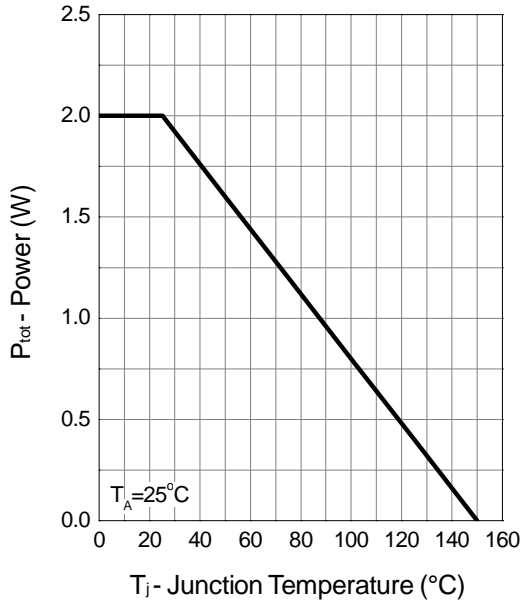
Gate Charge



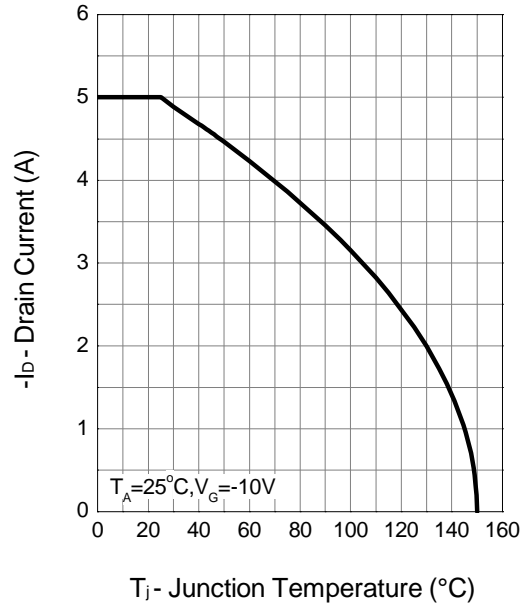
Typical Operating Characteristics (Cont.)

P-Channel

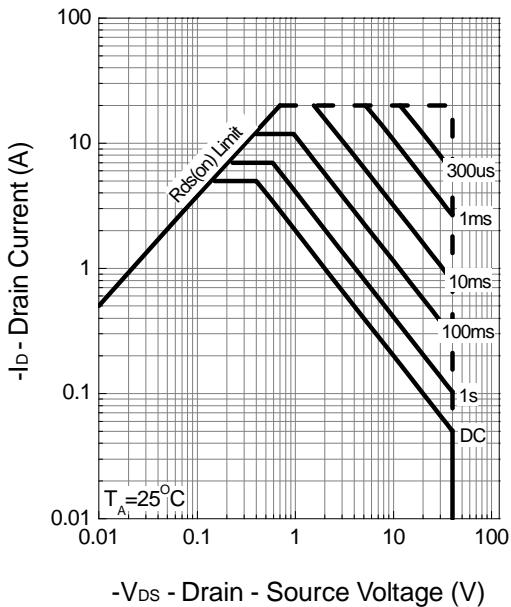
Power Dissipation



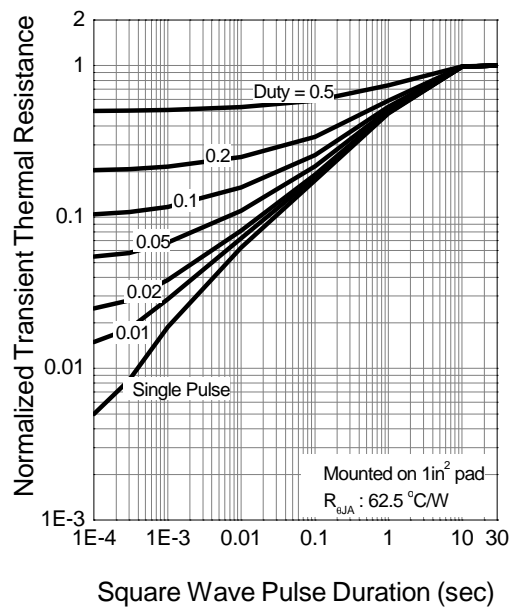
Drain Current



Safe Operation Area



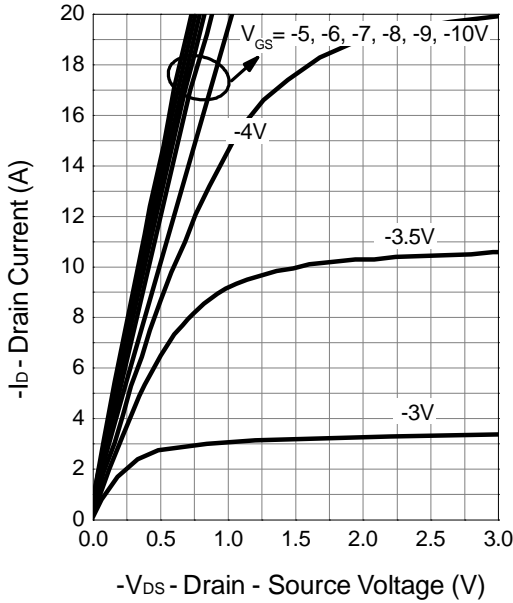
Thermal Transient Impedance



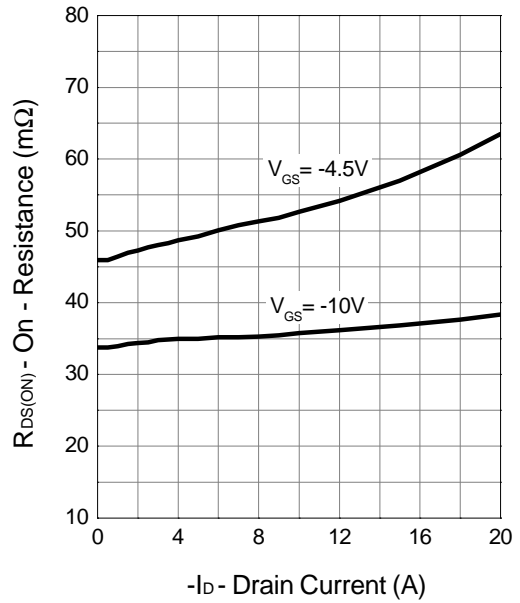
Typical Operating Characteristics (Cont.)

P-Channel

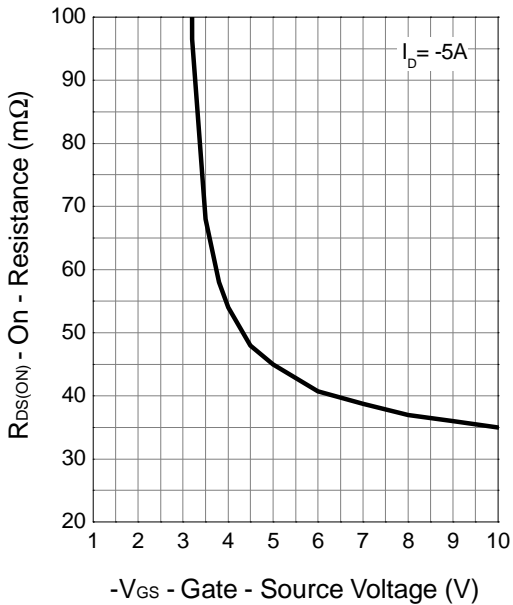
Output Characteristics



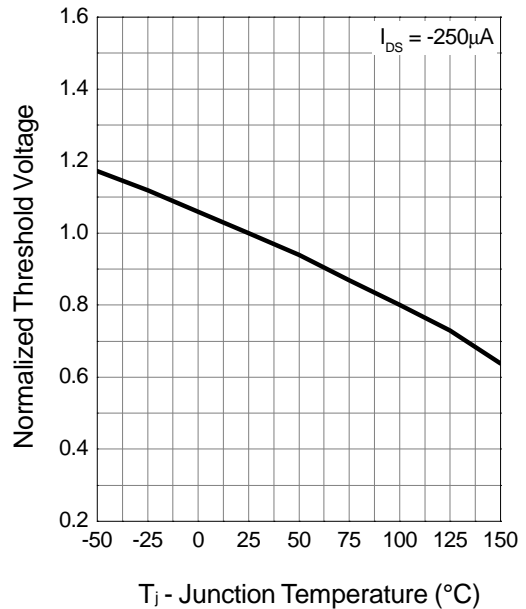
Drain-Source On Resistance



Drain-Source On Resistance



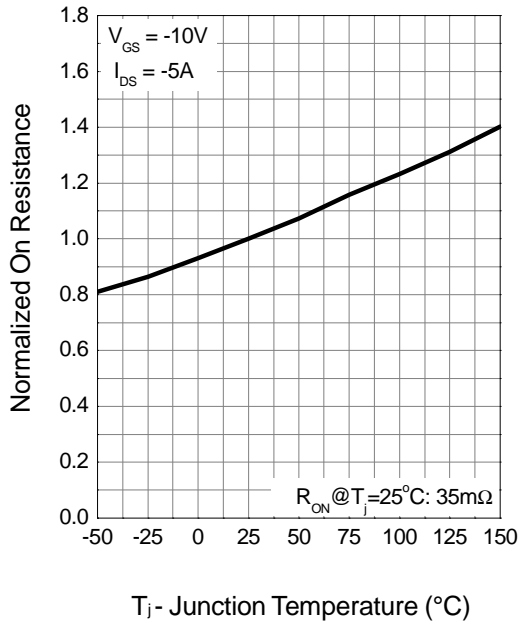
Gate Threshold Voltage



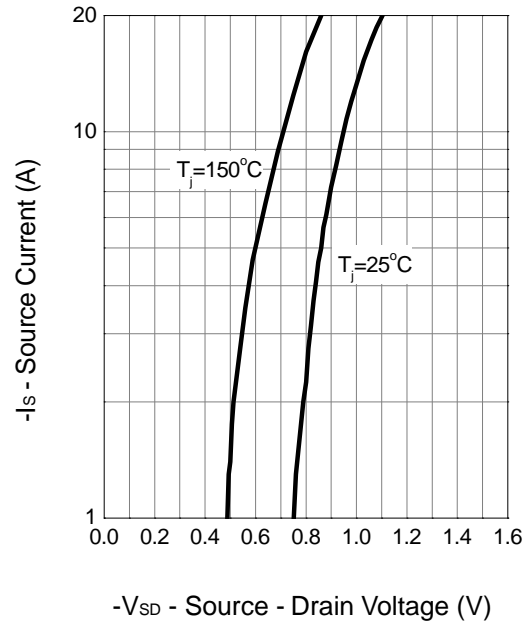
Typical Operating Characteristics (Cont.)

P-Channel

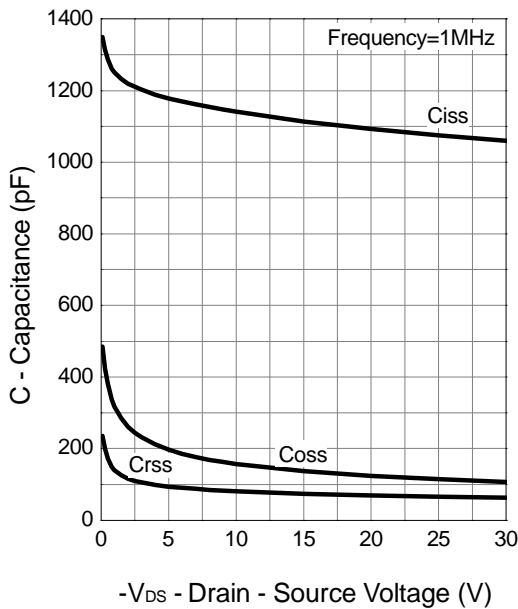
Drain-Source On Resistance



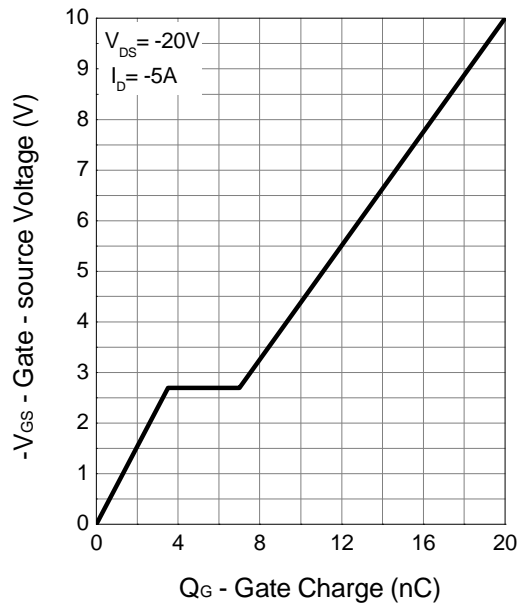
Source-Drain Diode Forward



Capacitance

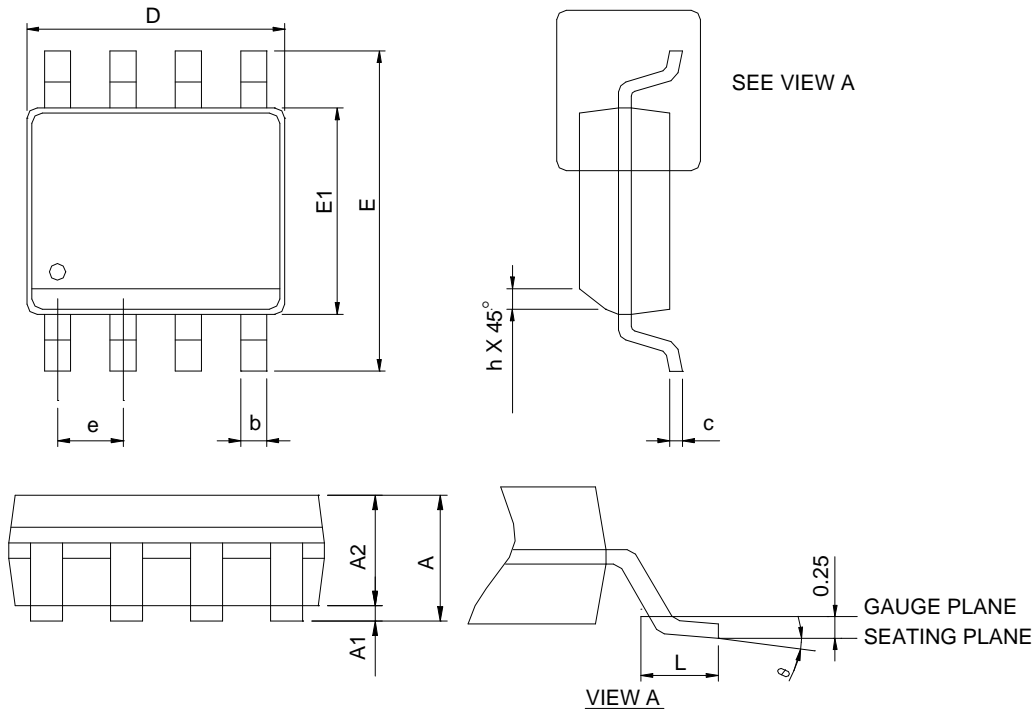


Gate Charge



Package Information

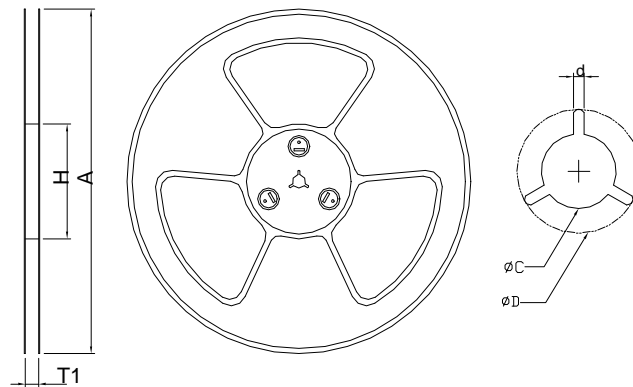
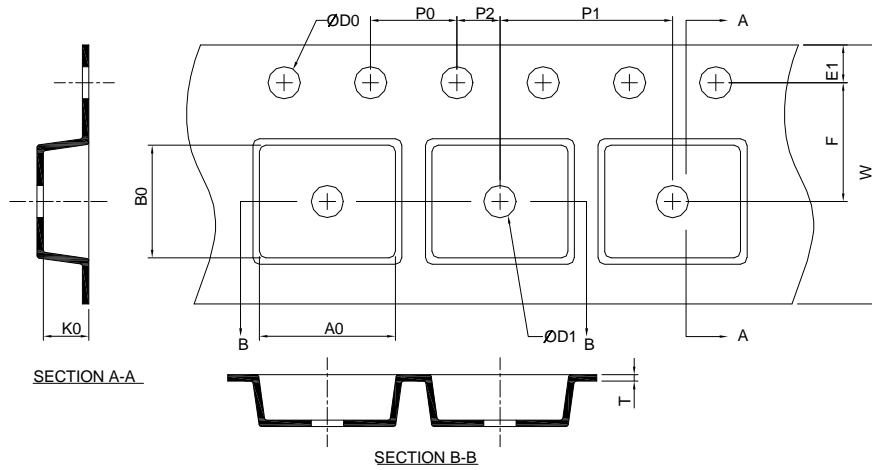
SOP-8



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

- Note: 1. Follow JEDEC MS-012 AA.
 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
 3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0 ± 2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0 ± 0.30	1.75 ± 0.10	5.5 ± 0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ± 0.10	8.0 ± 0.10	2.0 ± 0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40 ± 0.20	5.20 ± 0.20	2.10 ± 0.20

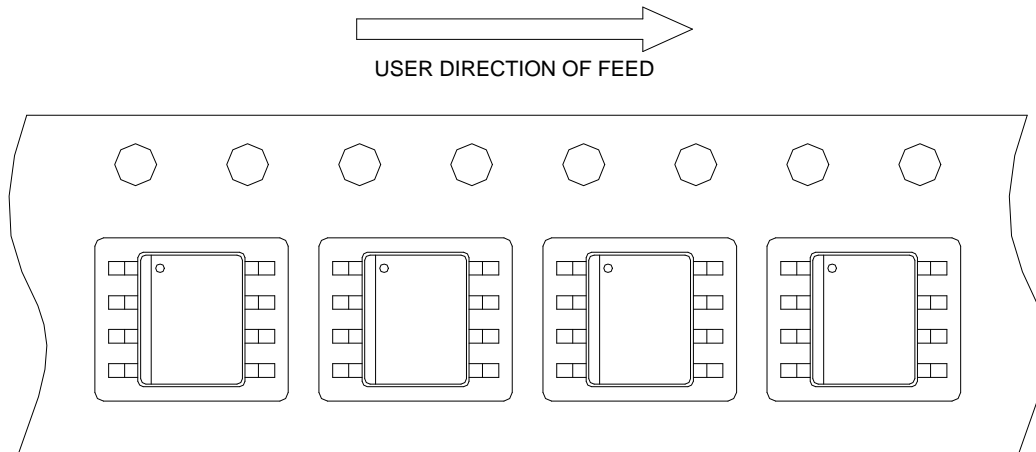
(mm)

Devices Per Unit

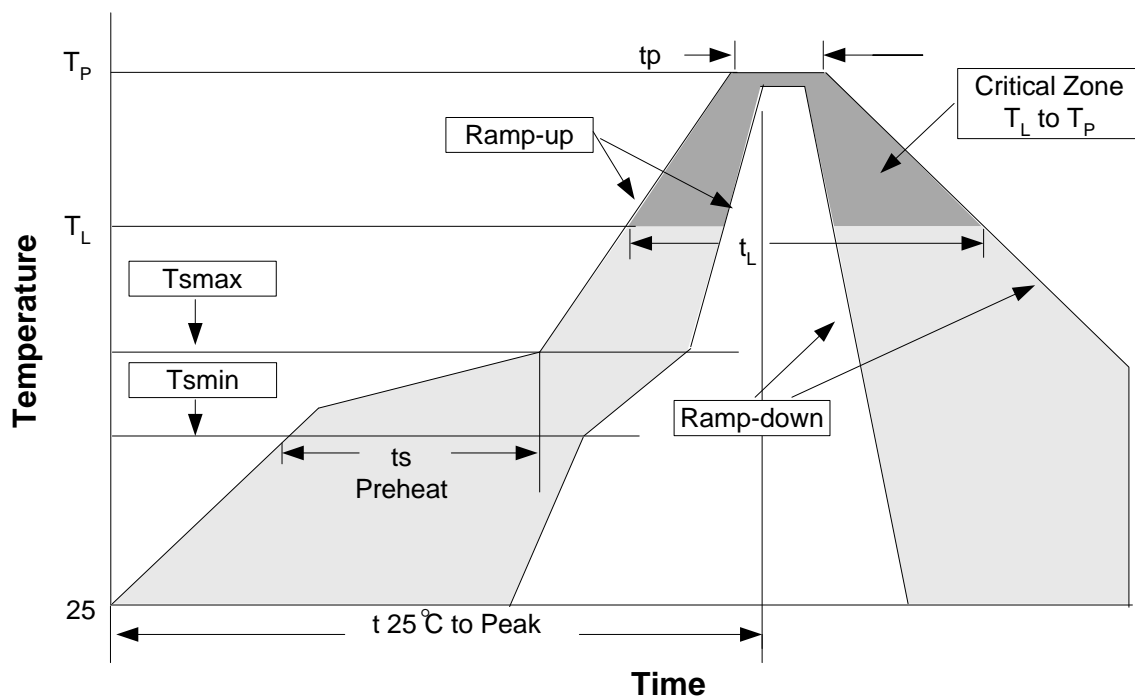
Package Type	Unit	Quantity
SOP-8	Tape & Reel	2500

Taping Direction Information

SOP-8



Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125°C
PCT	JESD-22-B, A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T _L to T _P)	3°C/second max.	3°C/second max.
Preheat		
- Temperature Min (T _{min})	100°C	150°C
- Temperature Max (T _{max})	150°C	200°C
- Time (min to max) (ts)	60-120 seconds	60-180 seconds
Time maintained above:		
- Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak/Classification Temperature (T _p)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Note: All temperatures refer to topside of the package. Measured on the body surface.

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

Customer Service

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