



## 32K × 8 CMOS STATIC RAM

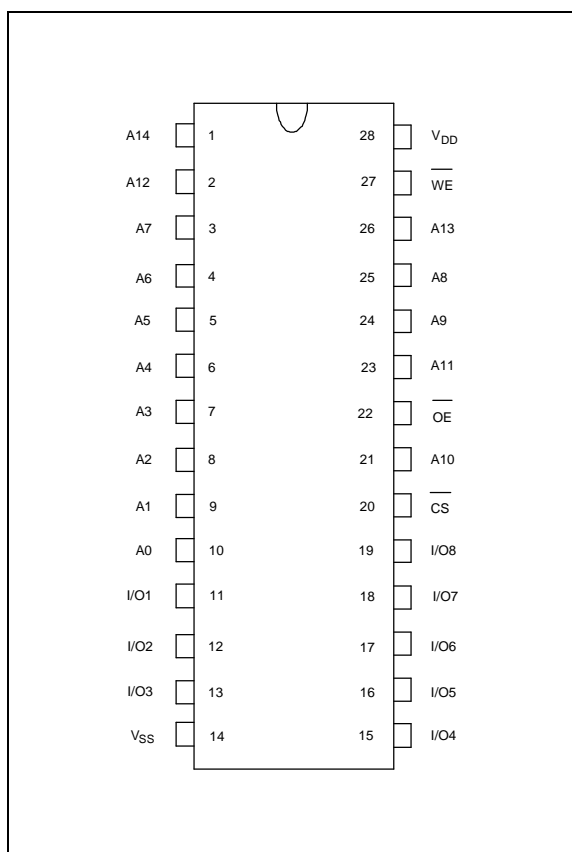
### GENERAL DESCRIPTION

The W24257 is a slow speed, low power CMOS static RAM organized as 32768 × 8 bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

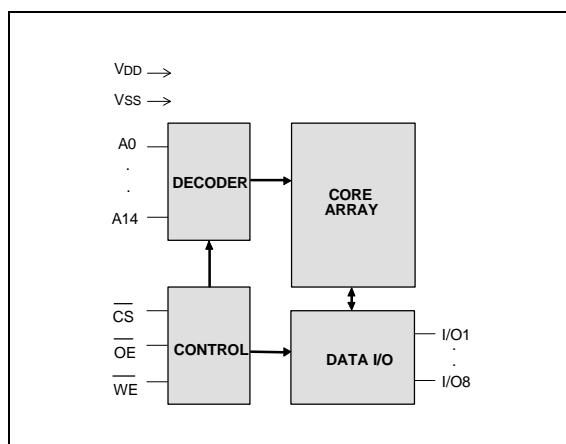
### FEATURES

- Low power consumption:
  - Active: 325 mW (max.)
  - Standby: 75 μW (max.) (LL-version)  
150 μW (max.) (L-version)
- Access time: 70 nS (max.)
- Single +5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 2V (min.)
- Packaged in 28-pin 600 mil DIP, 330 mil SOP, standard type one TSOP (8 mm x 13.4 mm )

### PIN CONFIGURATION



### BLOCK DIAGRAM



### PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A14	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
VDD	Power Supply
Vss	Ground



## TRUTH TABLE

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	MODE	I/O1 - I/O8	V <sub>DD</sub> CURRENT
H	X	X	Not Selected	High Z	ISB, ISB1
L	H	H	Output Disable	High Z	IDD
L	L	H	Read	Data Out	IDD
L	X	L	Write	Data In	IDD

## DC CHARACTERISTICS

### Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to V <sub>SS</sub> Potential	-0.5 to +7.0	V
Input/Output to V <sub>SS</sub> Potential	-0.5 to V <sub>DD</sub> +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

### Operating Characteristics

(V<sub>DD</sub> = 5V ±10%, V<sub>SS</sub> = 0V, T<sub>A</sub> = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Input Low Voltage	V <sub>IL</sub>	-	-0.5	-	+0.8	V	
Input High Voltage	V <sub>IH</sub>	-	+2.2	-	V <sub>DD</sub> +0.5	V	
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>DD</sub>	-2	-	+2	μA	
Output Leakage Current	I <sub>LO</sub>	V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>DD</sub> , $\overline{\text{CS}}$ = V <sub>IH</sub> (min.) or $\overline{\text{OE}}$ = V <sub>IH</sub> (min.) or $\overline{\text{WE}}$ = V <sub>IL</sub> (max.)	-2	-	+2	μA	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = +4.0 mA	-	-	0.4	V	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0 mA	2.4	-	-	V	
Operating Power Supply Current	I <sub>DD</sub>	$\overline{\text{CS}}$ = V <sub>IL</sub> (min.), I/O = 0 mA Cycle = min., Duty = 100%	-	-	65	mA	
Standby Power Supply Current	I <sub>SB</sub>	$\overline{\text{CS}}$ = V <sub>IH</sub> (min.) Cycle = min., Duty = 100%	-	-	3	mA	
	I <sub>SB1</sub>	$\overline{\text{CS}} \geq \text{VDD} - 0.2\text{V}$	LL	-	-	15	μA
			L	-	-	30	μA

Note: Typical characteristics are at V<sub>DD</sub> = 5V, T<sub>A</sub> = 25° C.



## CAPACITANCE

(V<sub>DD</sub> = 5V, T<sub>A</sub> = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	6	pF
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>OUT</sub> = 0V	8	pF

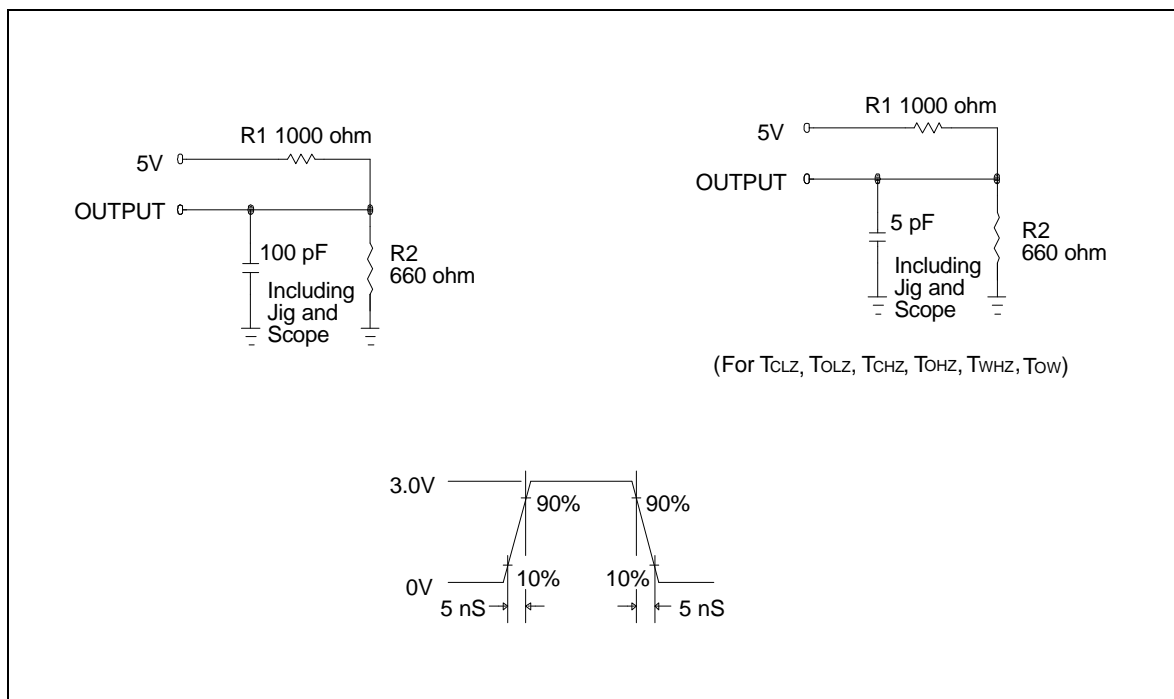
Note: These parameters are sampled but not 100% tested.

## AC CHARACTERISTICS

### AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	C <sub>L</sub> = 100 pF, I <sub>OH</sub> /I <sub>OL</sub> = -1 mA/4 mA

### AC Test Loads and Waveform





AC Characteristics, continued

(V<sub>DD</sub> = 5V ±10%, V<sub>SS</sub> = 0V, T<sub>A</sub> = 0 to 70° C)**Read Cycle**

PARAMETER	SYM.	W24257-70		UNIT
		MIN.	MAX.	
Read Cycle Time	TRC	70	-	nS
Address Access Time	TAA	-	70	nS
Chip Select Access Time	TACS	-	70	nS
Output Enable to Output Valid	TAOE	-	35	nS
Chip Selection to Output in Low Z	TCLZ*	10	-	nS
Output Enable to Output in Low Z	TOLZ*	5	-	nS
Chip Deselection to Output in High Z	TCHZ*	-	30	nS
Output Disable to Output in High Z	TOHZ*	-	30	nS
Output Hold from Address Change	TOH	10	-	nS

\* These parameters are sampled but not 100% tested

**Write Cycle**

PARAMETER	SYM.	W24257-70		UNIT
		MIN.	MAX.	
Write Cycle Time	TWC	70	-	nS
Chip Selection to End of Write	TCW	60	-	nS
Address Valid to End of Write	TAW	60	-	nS
Address Setup Time	TAS	0	-	nS
Write Pulse Width	TWP	45	-	nS
Write Recovery Time	$\overline{CS}$ , $\overline{WE}$ TWR	0	-	nS
Data Valid to End of Write	TDW	30	-	nS
Data Hold from End of Write	TDH	0	-	nS
Write to Output in High Z	TWHZ*	-	30	nS
Output Disable to Output in High Z	TOHZ*	-	30	nS
Output Active from End of Write	TOW	0	-	nS

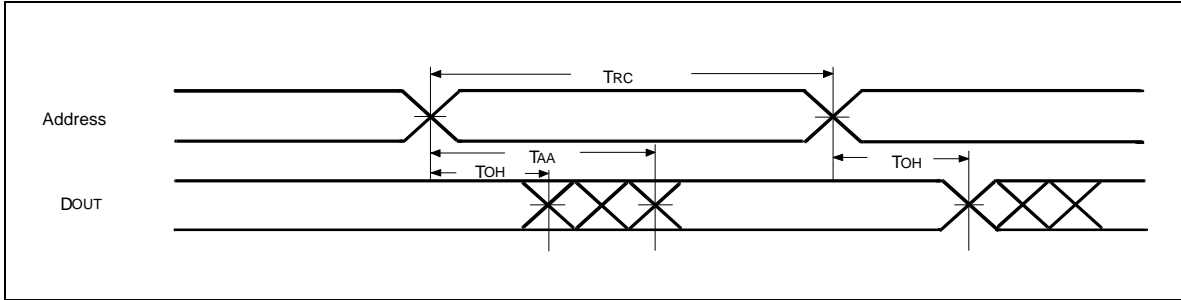
\* These parameters are sampled but not 100% tested



**TIMING WAVEFORMS**

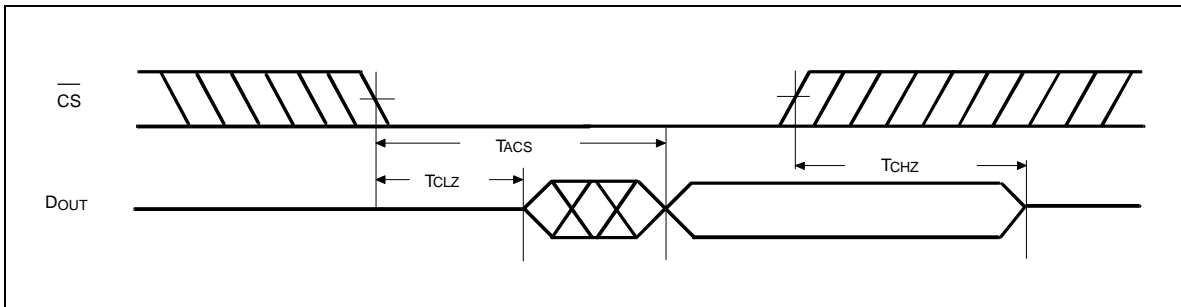
**Read Cycle 1**

**(Address Controlled)**



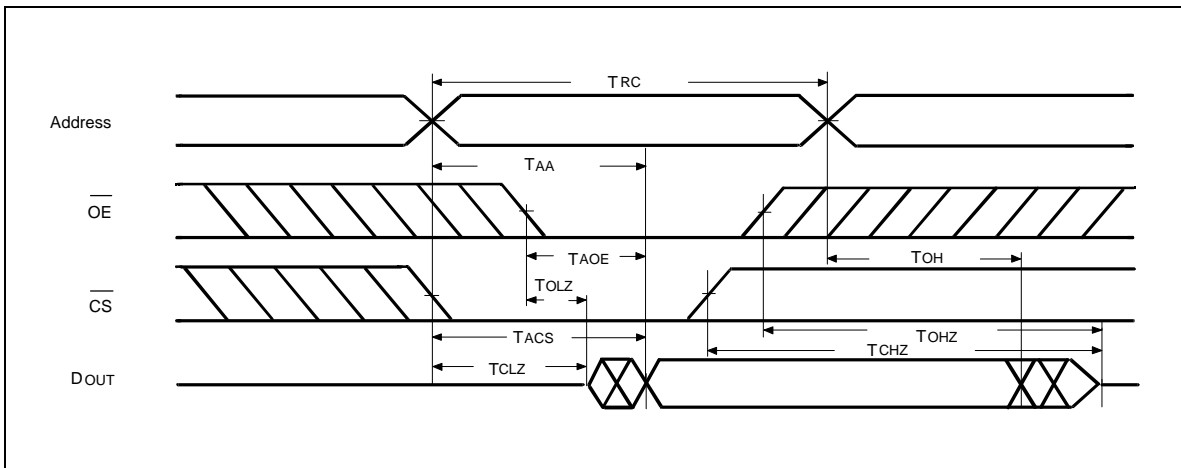
**Read Cycle 2**

**(Chip Select Controlled)**



**Read Cycle 3**

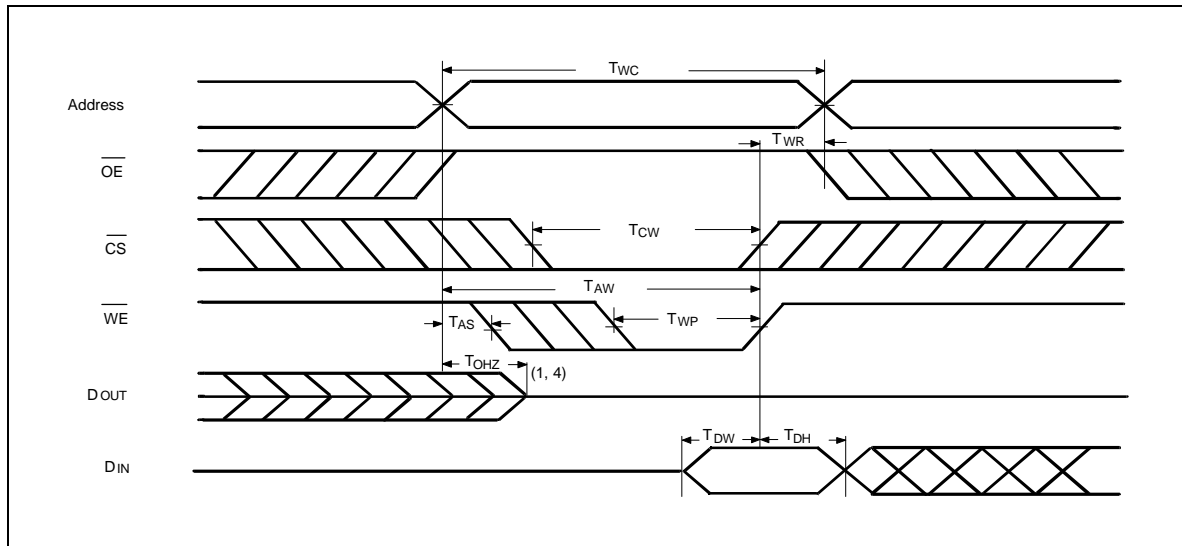
**(Output Enable Controlled)**





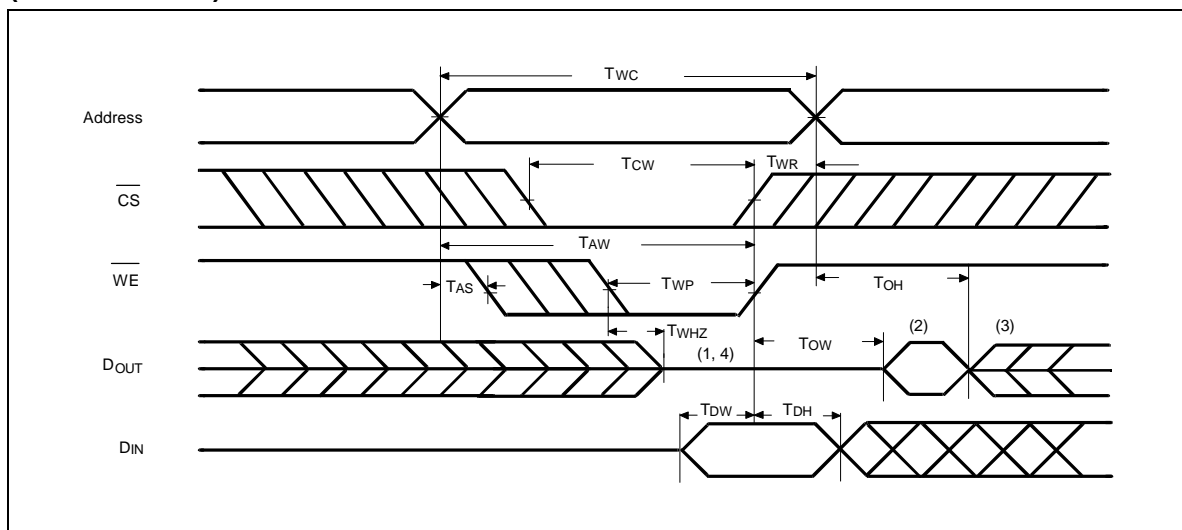
Timing Waveforms, continued

**Write Cycle 1**



**Write Cycle 2**

( $\overline{OE} = V_{IL}$  Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured  $\pm 500$  mV from steady state with  $C_L = 5$  pF. This parameter is guaranteed but not 100% tested.



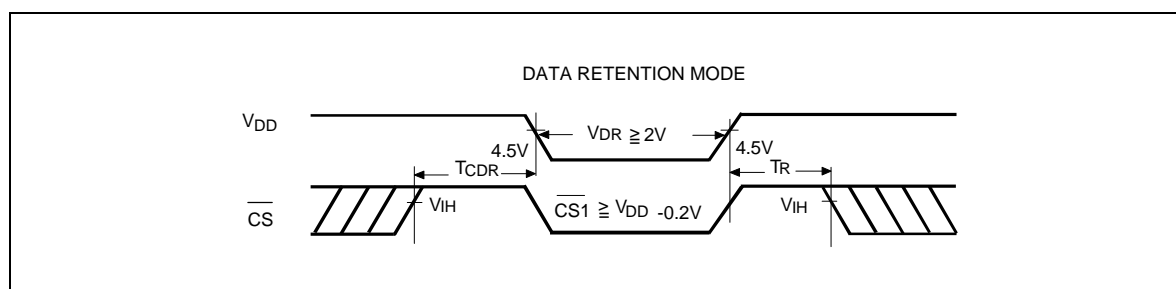
## DATA RETENTION CHARACTERISTICS

(T<sub>A</sub> = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
V <sub>DD</sub> for Data Retention	V <sub>DR</sub>	$\overline{CS} \geq V_{DD} - 0.2V$	2.0	-	-	V	
Data Retention Current	I <sub>DDDR</sub>	$\overline{CS} \geq V_{DD} - 0.2V$ V <sub>DD</sub> = 3V	LL	-	-	15	μA
			L	-	-	30	μA
Chip Deselect to Data Retention Time	T <sub>CDR</sub>	See data retention waveform	0	-	-	nS	
Operation Recovery Time	T <sub>R</sub>	waveform	TRC*	-	-	nS	

TRC\* = Read Cycle Time

## DATA RETENTION WAVEFORM



## ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W24257-70LL	70	65	15	600 mil DIP
W24257-70L	70	65	30	600 mil DIP
W24257S-70LL	70	65	15	330 mil SOP
W24257S-70L	70	65	30	330 mil SOP
W24257Q-70LL	70	65	15	Standard type one TSOP
W24257Q-70L	70	65	30	Standard type one TSOP

Notes:

- Winbond reserves the right to make changes to its products without prior notice.
- Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.



**PACKAGE DIMENSIONS**

**28-pin P-DIP**

Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A <sub>1</sub>	0.010	—	—	0.25	—	—
A <sub>2</sub>	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B <sub>1</sub>	0.058	0.060	0.064	1.47	1.52	1.63
C	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.460	1.470	—	37.08	37.34
E	0.590	0.600	0.610	14.99	15.24	15.49
E <sub>1</sub>	0.540	0.545	0.550	13.72	13.84	13.97
e <sub>1</sub>	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e <sub>A</sub>	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.090	—	—	2.29

**Notes:**

1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

**28-pin SO Wide Body**

Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.112	—	—	2.85
A <sub>1</sub>	0.004	—	—	0.10	—	—
A <sub>2</sub>	0.093	0.098	0.103	2.36	2.49	2.62
b	0.014	0.016	0.020	0.36	0.41	0.51
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	0.713	0.733	—	18.11	18.62
E	0.326	0.331	0.336	8.28	8.41	8.53
Ⓜ	0.044	0.050	0.056	1.12	1.27	1.42
H <sub>L</sub>	0.453	0.465	0.477	11.51	11.81	12.12
L	0.028	0.036	0.044	0.71	0.91	1.12
L <sub>E</sub>	0.059	0.067	0.075	1.50	1.70	1.91
S	—	—	0.047	—	—	1.19
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

**Notes:**

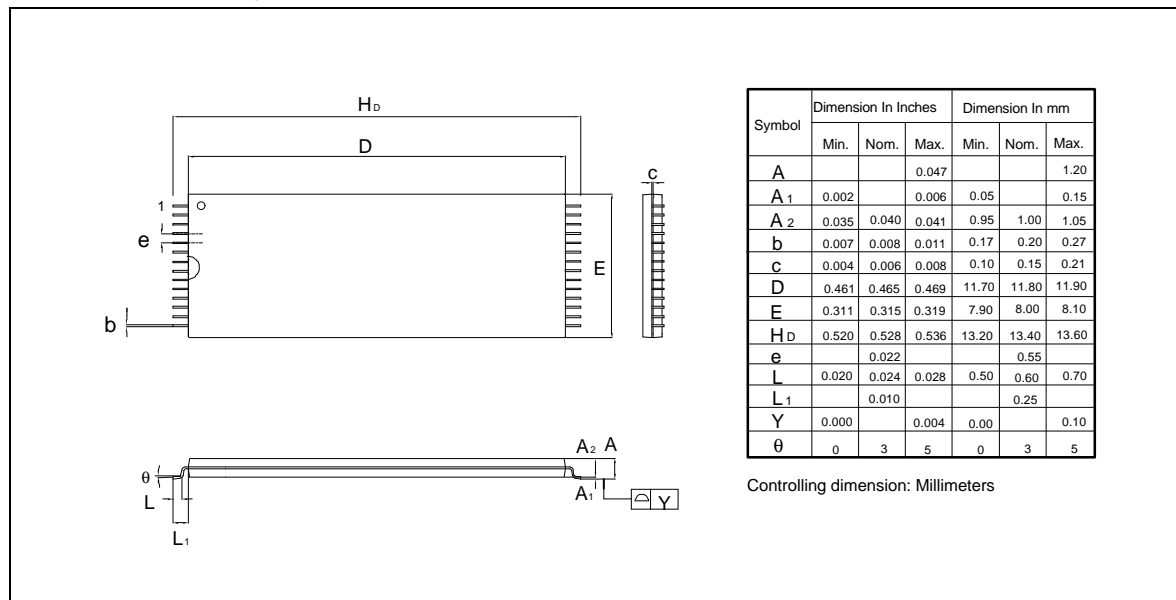
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension b does not include dambar protrusion/intrusion.
3. Dimension D & E include mold mismatch and determined at the mold parting line.
4. Controlling dimension: Inches.
5. General appearance spec should be based on final visual inspection spec.





Package Dimensions, continued

**28-pin Standard Type One TSOP**





## VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A12	Nov. 1999	1, 2, 7	Change the IDD, ISB, ISB1
		4, 7	Remove the W24257-10 spc.



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Note: All data and specifications are subject to change without notice.