SIEMENS

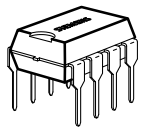
Control IC for Switched-Mode Power Supplies using MOS-Transistors

TDA 4605-2

Bipolar IC

Features

- Fold-back characteristics provides overload protection for external components
- Burst operation under secondary short-circuit condition implemented
- Protection against open or a short of the control loop
- Switch-off if line voltage is too low (undervoltage switch-off)
- Line voltage depending compensation of fold-back point
- Soft-start for quiet start-up without noise generated by the transformer
- Chip-over temperature protection implemented (thermal shutdown)
- On-chip ringing suppression circuit against parasitic oscillations of the transformer



P-DIP-8-1

Type	Ordering Code	Package
TDA 4605-2	Q67000-A5020	P-DIP-8-1

The IC TDA 4605-2 controls the MOS-power transistor and performs all necessary regulation and monitoring functions in free running flyback converters. Because of the fact that a wide load range is achieved, this IC is applicable for consumer as well as industrial power supplies.

The serial circuit and primary winding of the flyback transformer are connected in series to the input voltage. During the switch-on period of the transistor, energy is stored in the transformer. During the switch-off period the energy is fed to the load via the secondary winding. By varying switch-on time of the power transistor, the IC controls each portion of energy transferred to the secondary side such that the output voltage remains nearly independent of load variations. The required control information is taken from the input voltage during the switch-on period and from a regulation winding during the switch-off period. A new cycle will start if the transformer has transferred the stored energy completely into the load.

In the different load ranges the switched-mode power supply (SMPS) behaves as follow:

No load operation

The power supply is operating in the burst mode at typical 20 to 40 kHz. The output voltage can be a little bit higher or lower than the nominal value depending of the design of the transformer and the resistors of the control voltage divider.

Nominal operation

The switching frequency is reduced with increasing load and decreasing AC-voltage. The duty factor primarily depends on the AC-voltage.

The output voltage is only dependent on the load.

Overload point

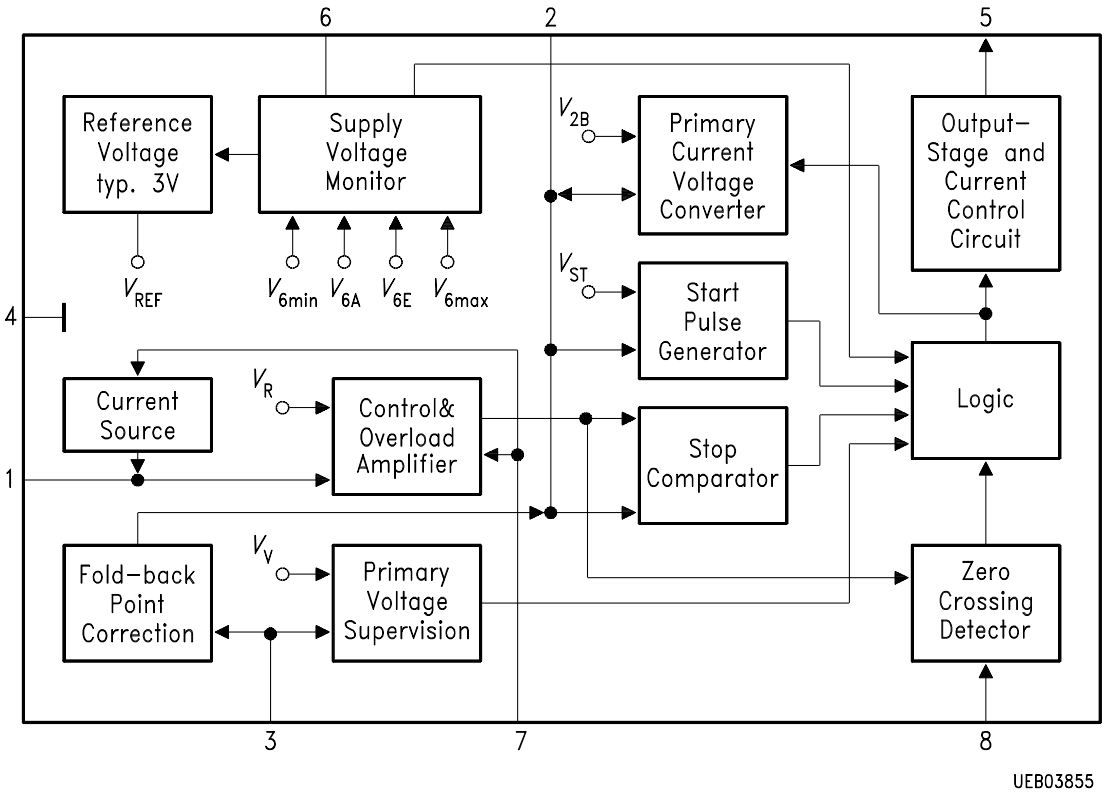
Maximal output power is available at this point of the output characteristic.

Overload

The energy transferred per operation cycle is limited at the top. Therefore the output voltages declines by secondary overloading.

Pin Definitions and Functions

Pin No.	Function
1	**Information Input Concerning Secondary Voltage.** By comparing the regulating voltage - obtained from the regulating winding of the transformer - with the internal reference voltage, the output impulse width on pin 5 is adjusted to the load of the secondary side (normal load, overload, short-circuit, no load).
2	**Information Input Regarding the Primary Current.** The primary current rise in the primary winding is simulated at pin 2 as a voltage rise by means of external RC-circuit. If a voltage level is reached which is derived from the control voltage at pin 1, the output impulse at pin 5 is terminated. The RC-circuit is used to set the maximum power of the foldback point.
3	**Input for Primary Voltage Monitoring:** In the normal operation V_3 is moving between the thresholds V_{3H} and V_{3L} ($V_{3H} > V_3 > V_{3L}$). $V_3 < V_{3L}$: SMPS is switched OFF (line voltage too low). $V_3 > V_{3H}$: Compensation of the overload point regulation (controlled by pin 2) starts at $V_{3H} : V_{3L} = 1.7$.
4	**Ground**
5	**Output:** Push-pull output for charging or discharging the gate capacity of the power MOSFET-transistor.
6	**Supply Voltage Input.** From the voltage at pin 6 a stable internal reference voltage V_{REF} and the switching thresholds V_{6A} , V_{6E} , $V_{6\,max}$ and $V_{6\,min}$ for the supply voltage detector are derived. If $V_6 > V_{6E}$ then V_{REF} is switched on. The reference voltage will be switched off if $V_6 < V_{6A}$. In addition the logic is only enable, for $V_{6\,min} < V_6 < V_{6\,max}$.
7	**Input for Soft-Start and Integrator Circuit.** The capacitor connected to ground causes a slow increase of the duration of the output pulse during start-up and an integrating response of the control amplifier.
8	**Input for the Feedback of the Oscillator.** After the oscillations of the SMPS started, every transition of the feedback voltage through zero (falling edge) triggers an output pulse at pin 5. The trigger threshold is at + 50 mV typical.



Block Diagram

Circuit Description

Application Circuit

The application circuit shows a flyback converter for video recorders with an output power rating of 70 W. The circuit is designed as a wide-range power supply for AC-line voltages of 180 to 264 V. The AC-input voltage is rectified by the bridge rectifier GR1 and smoothed by C_1 . The NTC limits the rush-in current.

The IC includes an internal circuit to avoid the turn-on of the power transistor T1 because of static charges applied to the transistors gate, during the turn-off state of the IC. The resistor R_{13} helps to limit the spectrum of the radiated noise.

During the conductive phase of the power transistor T1 the current rise in the primary winding depends on the winding inductance and the mains voltage.

The network consisting of R_4-C_5 is used to create a model of the sawtooth shaped rise of the collector current. The resulting control voltage is fed into pin 2 of the IC. The RC-time constant given by R_4-C_5 must be designed that way that driving the transistor core into saturation is avoided.

The ratio of the voltage divider R_{10}/R_{11} is fixing a voltage level threshold. Below this threshold the switching power supply shall stop operation because of the low mains voltage. The control voltage present at pin 3 also determines the correction current for the foldback point.

This current added to the current flowing through R_4 and represents an additional charge to C_5 in order to reduce the turn-on phase of T1. This is done to stabilize the fold-back point even under higher mains voltages.

The control of the switched-mode power supply is done by means of a control voltage applied to pin 1. The control voltage of winding n_1 during the off-period of T1 is rectified by D3 smoothed by C_6 and stepped down at an adjustable ratio by R_5 , R_6 and R_7 . The primary peak current, is adjusted by the IC so that the voltage applied across the control winding, and hence the output voltages, are at the desired level.

When the energy stored in the transformer is transferred into the load the control voltage passes through zero. The IC detects the zero crossing via the series R_9 connected to pin 8. But zero crossings of the control voltage can also be produced by ringing of the transformer after the turn-off of the power transistor for T1 or when a short-circuit is applied to the output of the SMPS.

The capacitor C_8 is connected to pin 7. During the start-up phase this capacitor assures pulses with a shorter duty cycle in order to keep the operating frequency outside the audible frequency range.

On the secondary side of the transformer 3 output voltages are produced using the windings n_2 to n_5 , rectified by D4 to D6 and smoothed by C_9 to C_{11} . The resistor R_{12} is used as a bleeder resistor, the resistors with implemented fuse R_{15} and R_{16} protect the rectifies against short circuits in the output circuits, which are designed to supply only small loads.

Block Diagram

Pin 1

In the control and overload amplifier the control voltage applied to this pin is compared with a stable internal reference voltage V. The output signal of this stage is fed to the "stop" comparator. If the control voltage is rather small at pin 1 an additional current is added by means of current source which is controlled according the level at pin 7. This additional current is virtually reducing the control voltage present at pin 1.

Pin 2

A voltage proportional to the drain current of the switching transistor is generated by means of an external RC-combination in conjunction with the internal functional block **primary current / voltage converter**. The output of this converter is controlled by the internal functional block "logic" and is also connected to the internal reference voltage V_{2B} . If the voltage V_2 exceeds the output voltage of the "control and overload amplifier" the stop comparator will reset the control logic. Consequently the output of pin 5 is switched to low potential. Further inputs for the logic stage are the outputs of the start impulse generator with the stable reference potential V_{ST} , the supply voltage monitoring circuit as well as the primary voltage supervision circuit.

Pin 3

The primary voltage applied here via a voltage divider is used to stabilize the fold-back point. In addition the logic is disable if - in comparison with the internal reference voltage V_V - a mains undervoltage condition is detected.

Pin 4

Ground

Pin 5

In the output stage the output signals from the "logic" block are converted into driving signals suitable for power MOS-transistors.

Pin 6

From the supply voltage V_6 applied to this pin internally a stable reference voltage V_{REF} as well as the switching threshold V_{6A} , V_{6E} , $V_{6\ max}$ and $V_{6\ min}$, for the supply voltage monitor section of the IC. All other inter reference value (V_R , V_{2B} , V_{ST} and V_v) are derived for V_{REF} . If $V_6 > V_{6E}$ the V_{REF} voltage source is switched on and the source is switched off if $V_6 < V_{6A}$. In addition the logic is enable only if $V_{6\ min} < V_6 < V_{6\ max}$.

Pin 7

By means of a resistor pin 7 is connected with the output of the control amplifier. If V_1 is approx. equal to the control voltage V_R the control amplifier has a proportional integrating control characteristics. The response of the control loop is derived from the capacitor connected to pin 7. If V_1 is equal to 0 V the control and overload amplifier is generating a ramp-up function using the capacitor connected to pin 7.

Pin 8

The zero crossing detector controlling the logic block recognizes the complete discharge of the energy stored in the transformator core by detecting the zero crossing the positive to negative voltage transition of the voltage at pin 8. This enables the logic for a new pulse. Parasitic oscillations occurring at the end of a pulse cannot lead to a new pulse because of an internal circuit which inhibits the zero detector for a certain dead time t_{UL} after the end of each pulse.

Start-Up Behaviour

The start-up behaviour of the application circuit (which is given on page 68) is explained in the diagrams on page 70 for a line voltage barely above the lower acceptable lower limit of the mains voltage. After applying the mains voltage at the time t_0 the following built up of different voltages can be seen:

- V_6 corresponding to the half-wave charge current over R_1
- V_2 to $V_{2\,max}$ (typically 6.6 V)
- V_3 to the value determined by the divider R_{10}/R_{11}

The current drawn by the IC in this case is less than 0.8 mA.

If V_6 reaches the threshold (at the time t_1 in the diagram), the IC internal reference voltage is switched on. The supply current drawn by the IC rises to 12 mA max.. The primary current/voltage converter reduces V_2 down to V_{2B} and the start pulse generator generates the start pulses from time point t_5 to t_6 in the diagram. The feedback to pin 8 starts the next pulse and so on. The width of all pulses including the start pulse are controlled by means of the control and overload amplifier. After turn on the IC is generating a signal at pin 7 which slowly ramping up. This signal is used to increase the duration of the output pulses slowly (soft-start function). The max. output pulse width is limited by means of the overload amplifier. If the feedback control voltage V_1 is increasing, the overload amplifier allows the generation of output pulses with a wider pulse width. The max. pulse width is reached at time t_2 in the diagram ($V_2 = V_{2S\,max}$). The IC is then operating at the fold-back point. Thereafter the peak values of V_2 decrease rapidly, because of the IC control range. The control loop is in a steady, operational state.

If the voltage V_6 falls below the switch-off threshold $V_{6\,min}$ before the foldback point is reached, the attempt to start the SMPS is aborted (pin 5 is switched to low). As the internal circuits of the IC remain switched on, V_6 further decreases to V_{6A} . The IC switches off; V_6 can rise again (time t_4 in the diagram) and new start-up attempt begins at time t_1 .

If the voltage level of the rectified mains voltage is reduced strongly under the influence of the applied load it can happen that V_3 is below the voltage level V_{3A} - please refer to the time t_3 in the diagram. This is because if an attempt is made to start the SMPS with a too low mains voltage. The internal primary voltage monitor circuit then clamps the voltage V_3 to the voltage level V_{3S} until the IC switches off ($V_6 < V_{6A}$). After this a new attempt to start the SMPS will begin at the time t_1 in the diagram.

Control Range, Overload and No-Load Behaviour

After the IC has started, it is operating in the control range. The voltage level at pin 1 is typically 400 mV. The gain of the control circuit consist of two parts: at first a fixed proportional part which is internally fixed and an integrating part which can be set by means of the external capacitor at pin 7. If the load is applied to the output of the SMPS, the control and overload amplifier allows wider pulses (V_5 = "H") .The peak voltage value at pin 2 increases up to $V_{2S\ max}$. If the secondary load is increased further the overload amplifier begins to reduce the pulse width of the output pulse. This point is referred to as the fold-back point of the power supply. Because of the fact that the IC supply voltage is directly proportional to the secondary voltage, the supply voltage V_6 will be reduced according to the behaviour of the control circuit under the overload condition. If V_6 falls below the value $V_{6\ min}$, the IC will operate in the burst mode. Because of the large time constant of the start-up circuit which is operating with half-wave rectification, only a small output power is transferred into the load during the secondary short-circuit of the SMPS. The overload amplifier reduces the output pulse width down to the pulse width t_{pk} . This pulse width must remain possible in order to permit the IC to start up without problems from the virtual short-circuit, which every switching on with V_1 = 0 is representing.

If no load is applied to the secondary side, the output pulses (V_5 = H) become shorter.

If the pulse width is reduced be low a certain internal limit the IC will suppress some of the output pulses. If the load is reduced further because of the decreasing duty cycle the measurement error of the rectifier network (R_8 , D3, C_6 of the application circuit) is increasing and therefore the secondary output voltage will increase, too. If the IC is operating with small pulse width of the output pulse the control amplifier applies an additional current to the control amplifier in order to reduce the output voltage. The value of the additional current depends on the size of the resistors R_5 , R_8 , R_7 . This can be used to compensate the increase of the secondary voltages.

Behaviour if the Chip Temperature Exceeds Predefined Limits

An integrated protection circuit against over temperature disables the internal logic if the chip temperature is too high. The internal logic automatically checks the chip temperature and restart the SMPS as soon as the temperature decreases to a permissible level.

Absolute Maximum Ratings

T_A = – 20 to 85 ˚C; all voltages relatives to V_{pp}

Parameter		Symbol	Limit Values		Unit	Remarks
			min.	max.		
Voltages	pin 1	V_1	– 0.3	3	V	
	pin 2	V_2	– 0.3		V	
	pin 3	V_3	– 0.3		V	
	pin 5	V_5	– 0.3	V_6	V	
	pin 6	V_6	– 0.3	20	V	Supply voltage
	pin 7	V_7	– 0.3		V	
Currents	pin 1	I_1		3	mA	
	pin 2	I_2		3	mA	
	pin 3	I_3		3	mA	
	pin 4	I_4	– 1.5		A	$t_p \leq 50$ µs; v ≤ 0.1*)
	pin 5	I_5	– 0.5	1.5	A	$t_p \leq 50$ µs; v ≤ 0.1
	pin 6	I_6		0.5	A	$t_p \leq 50$ µs; v ≤ 0.1
	pin 7	I_7		3	mA	
	pin 8	I_8	– 5	3	mA	
Junction temperature		T_j		125	˚C	
Storage temperature		T_{stg}	– 40	125	˚C	

Operating Range

Supply voltage	V_6	7.5	15.5	V	IC "on"
Ambient temperature	T_A	– 20	85	˚C	
Heat resistance					
Junction environment	$R_{th\ JE}$		100	K/W	
Junction package	$R_{th\ JG}$		70	K/W	measured at pin 4

*) t_p= pulse width
v= duty circle

Characteristics

T_A = 25 °C; V_S = 10 V

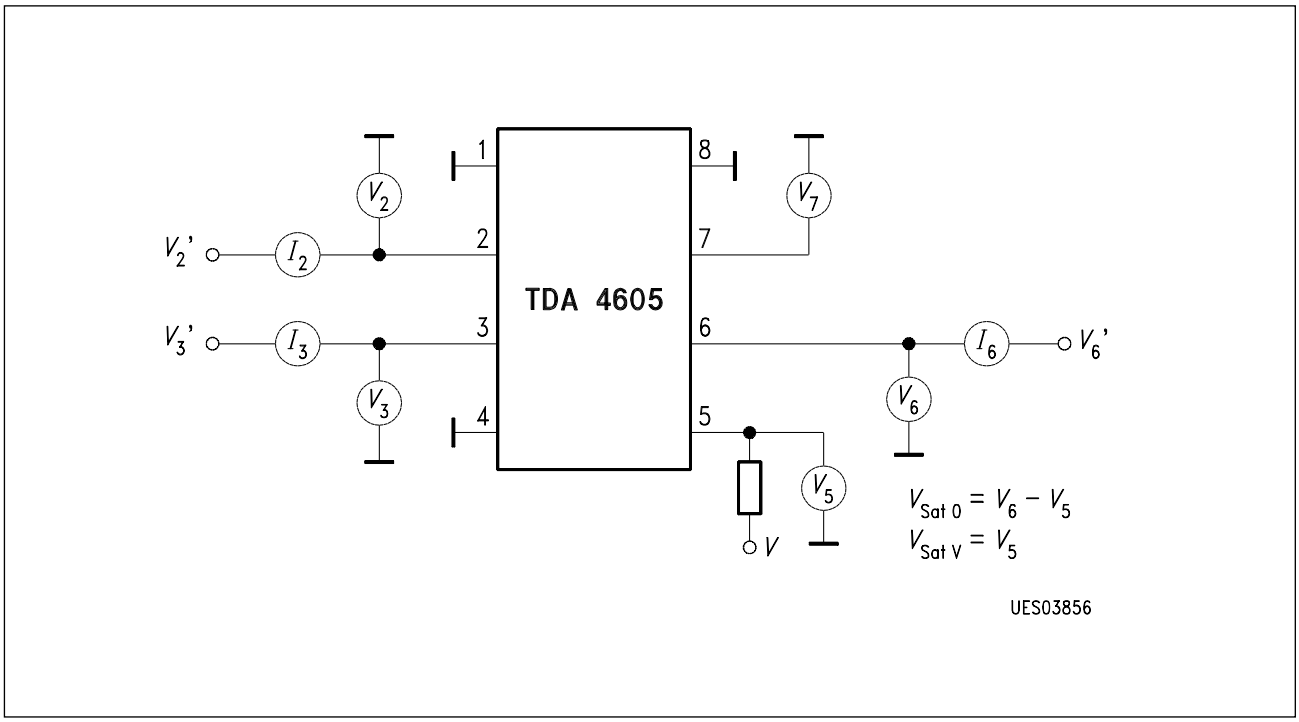
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Start-Up Hysteresis							
Start-up current drain	I_{6E0}		0.6	0.8	mA	$V_6 = V_{6E}$	1
Switch-on voltage	V_{6E}	11	12	13	V		1
Switch-off voltage	V_{6A}	4.5	5	5.5	V		1
Switch-on current	I_{6E1}		11		mA	$V_6 = V_{6E}$	1
Switch-off current	I_{6A1}		10		mA	$V_6 = V_{6A}$	1
Voltage Clamp (V_6 = 10 V, IC switched off)							
At pin 2 ($V_6 \leq V_{6E}$) At pin 3 ($V_6 \leq V_{6E}$)	$V_{2\ max}$ $V_{3\ max}$	5.6 5.6	6.6 6.6	8 8	V V	I_2 = 1 mA I_3 = 1 mA	1 1
Control Range							
Control input voltage	V_{1R}	390	400	410	mV		2
Voltage gain of the control circuit in the control range	$-V_R$		43		dB	V_R = d $(V_{2S} - V_{2B})$/– dV_1 f = 1 kHz	2
Primary Current Simulation Voltage							
Basic value	V_{2B}	0.97	1.00	1.03	V		2
Overload Range and Short-Circuit Operation							
Peak value in the range of secondary overload	V_{2O}	2.9	3.0	3.1	V	$V_1 = V_{1R}$ – 10 mV	2
Peak value in the range of secondary short-circuit operation	V_{2S}	2.2	2.4	2.6	V	V_1 = 0 V	2
Fold-Back Point Correction							
Fold-back point correction current	$-I_2$	300	500	650	µA	V_3 = 3.7 V	1

Characteristics (cont'd)
T_A = 25 °C; V_S = 10 V

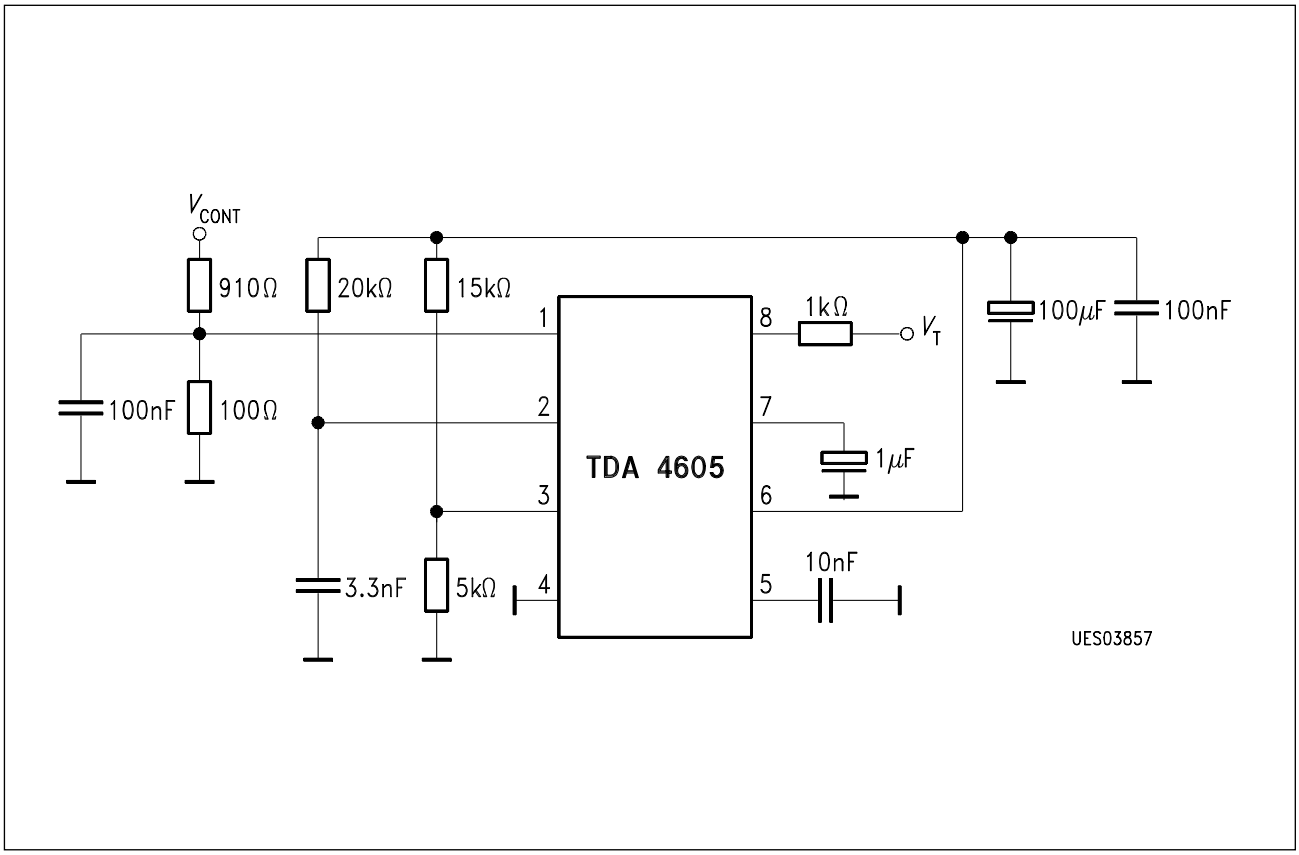
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Generally Valid Data (V_6 = 10 V)							
Voltage of the Zero Transition Detector							
Positive clamping voltage	V_{8P}		0.75		V	I_8 = 1 mA	2
Negative clamping voltage	V_{8N}		– 0.2		V	I_8 = – 1 mA	2
Threshold value	V_{8S}	40	50		mV		2
Suppression of transformer ringing	t_{UL}	4	4.5	5.5	µs		2
Input current	$-I_8$	0		4	µA	V_8 = 0	
Push-Pull Output Stage							
Saturation voltages							
Pin 5 sourcing	V_{Sat0}		1.5	2.0	V	I_5 = – 0.1 A	1
Pin 5 sinking	V_{SatV}		1.0	1.2	V	I_5 = + 0.1 A	1
Pin 5 sinking	V_{SatV}		1.4	1.8	V	I_5 = + 0.5 A	1
Output Slew Rate							
Rising edge	+ dV_5/dt		20		V/µs		2
Falling edge	+ dV_5/dt		50		V/µs		2
Reduction of Control Voltage							
Current to reduce the control voltage	$-I_1$		50		µA	V_7 = 1.1 V	

Characteristics (cont'd)
T_A = 25 °C; V_S = 10 V

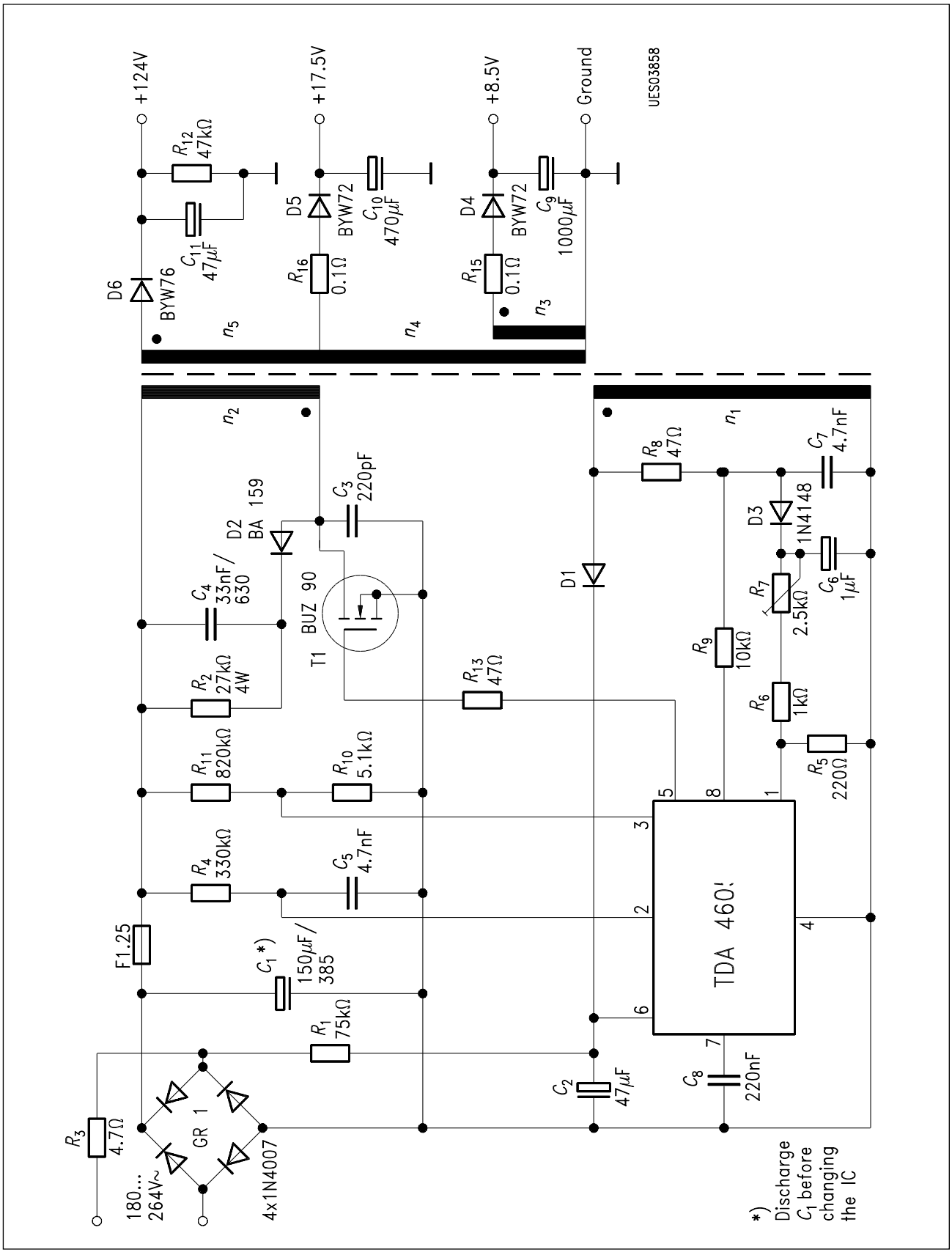
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Protection Circuit							
Undervoltage protection for V_6 : voltage at pin 5 = $V_{5\ min}$ if $V_6 < V_{6\ min}$	$V_{6\ min}$	7.0	7.25	7.5	V		2
Undervoltage protection for V_6 : voltage at pin 5 = $V_{5\ min}$ if $V_6 > V_{6\ max}$	$V_{6\ max}$	15.5	16	16.5	V		2
Undervoltage protection for V_{AC} : voltage at pin 5 = $V_{5\ min}$ if $V_3 < V_{3A}$	V_{3A}	985	1000	1015	mV	V_2 = 0 V	1
Over temperature at the given chip the temperature IC will switch V_5 to $V_{5\ min}$	T_j		150		°C		2
Voltage at pin 3 if one of the protection functions was triggered; (V_3 will be clamped until $V_6 < V_{6A}$)	V_{3Sat}		0.4	0.8	V	I_3 = 750 µA	1
Current drain during burst operation	I_6		8		mA	$V_3 = V_2$ = 0 V	1



Test Circuit 1

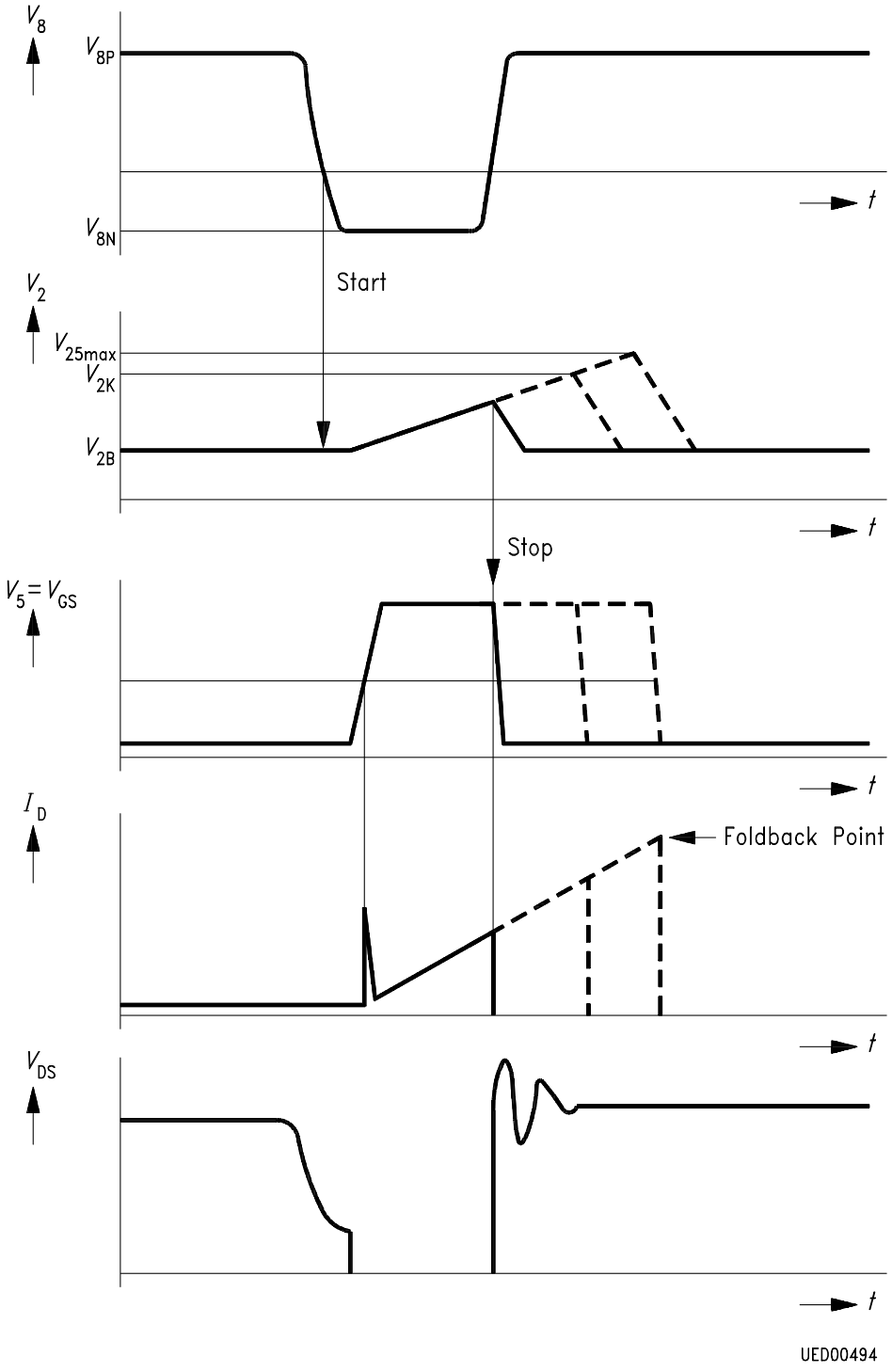


Test Circuit 2



Application Circuit

Diagrams


V_8
V_{8P}
V_{8N}
t
Start
V_2
V_{25max}
V_{2K}
V_{2B}
t
Stop
$V_5 = V_{GS}$
t
I_D
Foldback Point
t
V_{DS}
t
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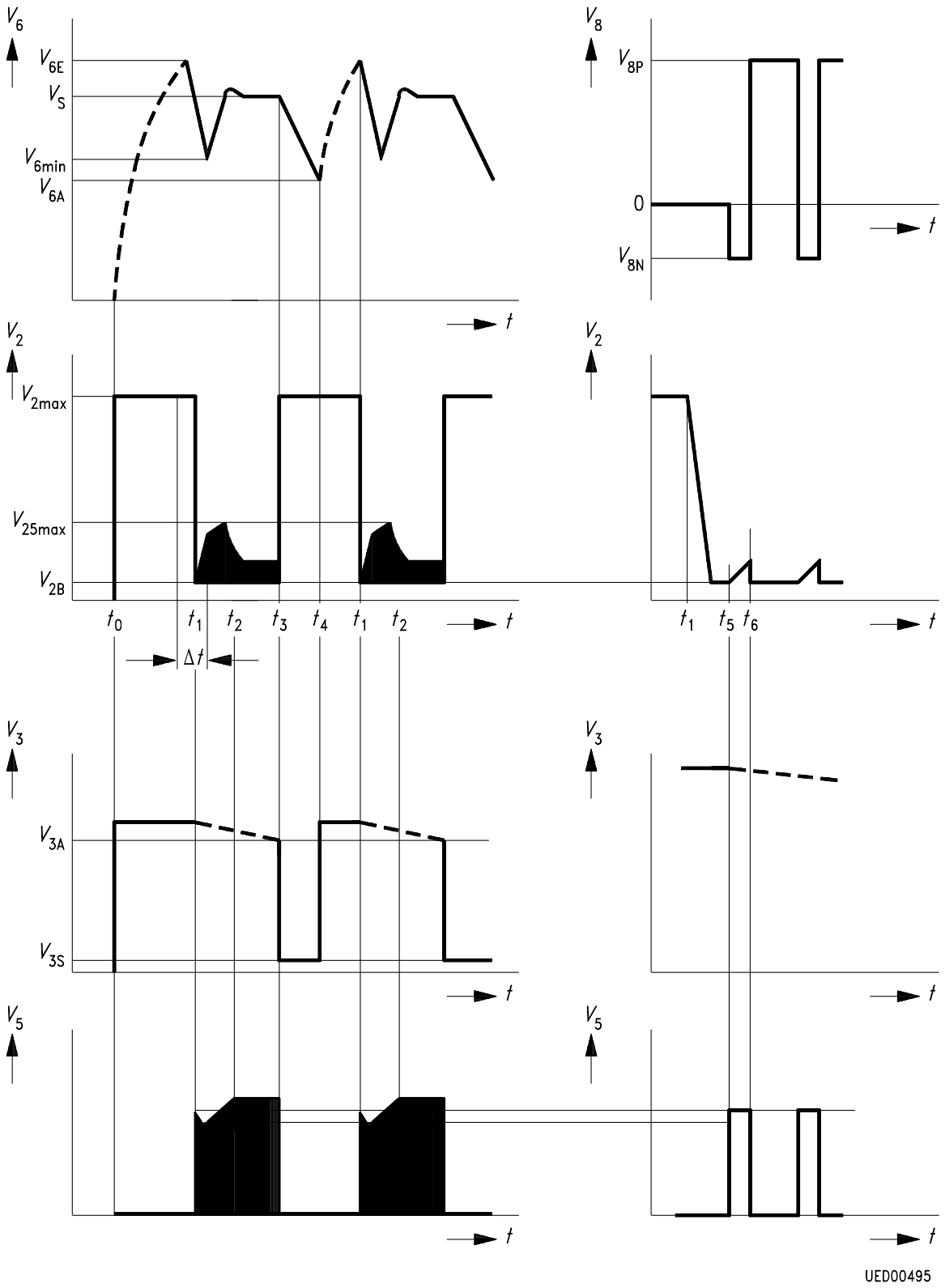
V_6
V_{6E}
V_S
V_{6min}
V_{6A}
t
V_8
V_{8P}
0
V_{8N}
t
V_2
V_{2max}
V_{25max}
V_{2B}
t_0 t_1 t_2 t_3 t_4 t_1 t_2
Δt
t
V_2
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t
V_3
V_{3A}
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t
V_3
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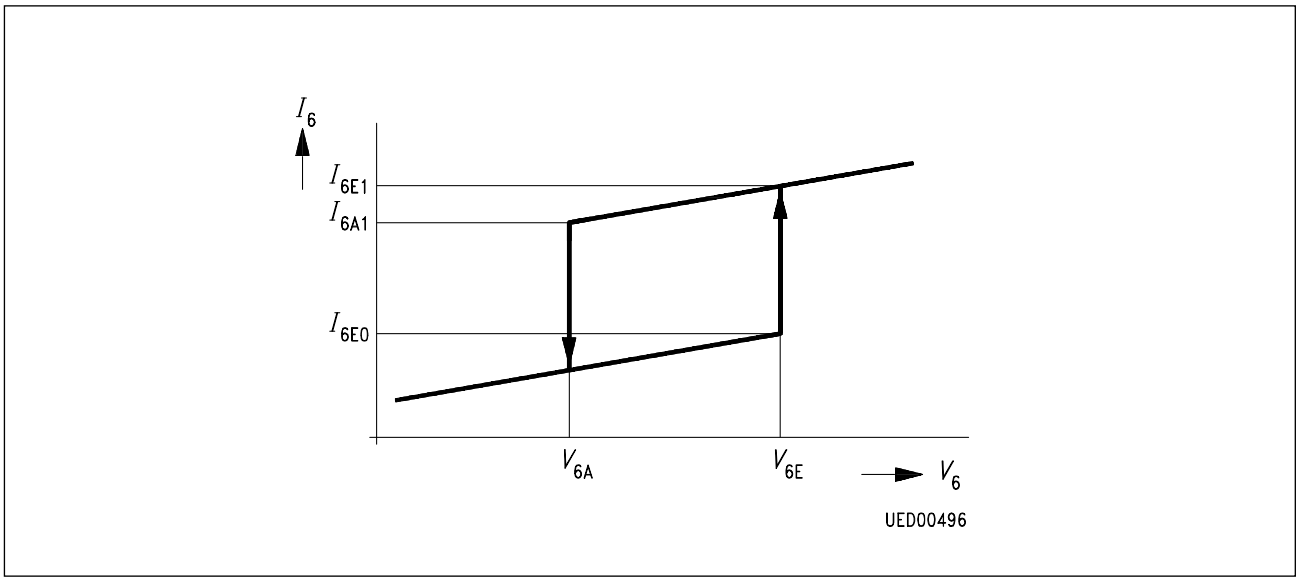
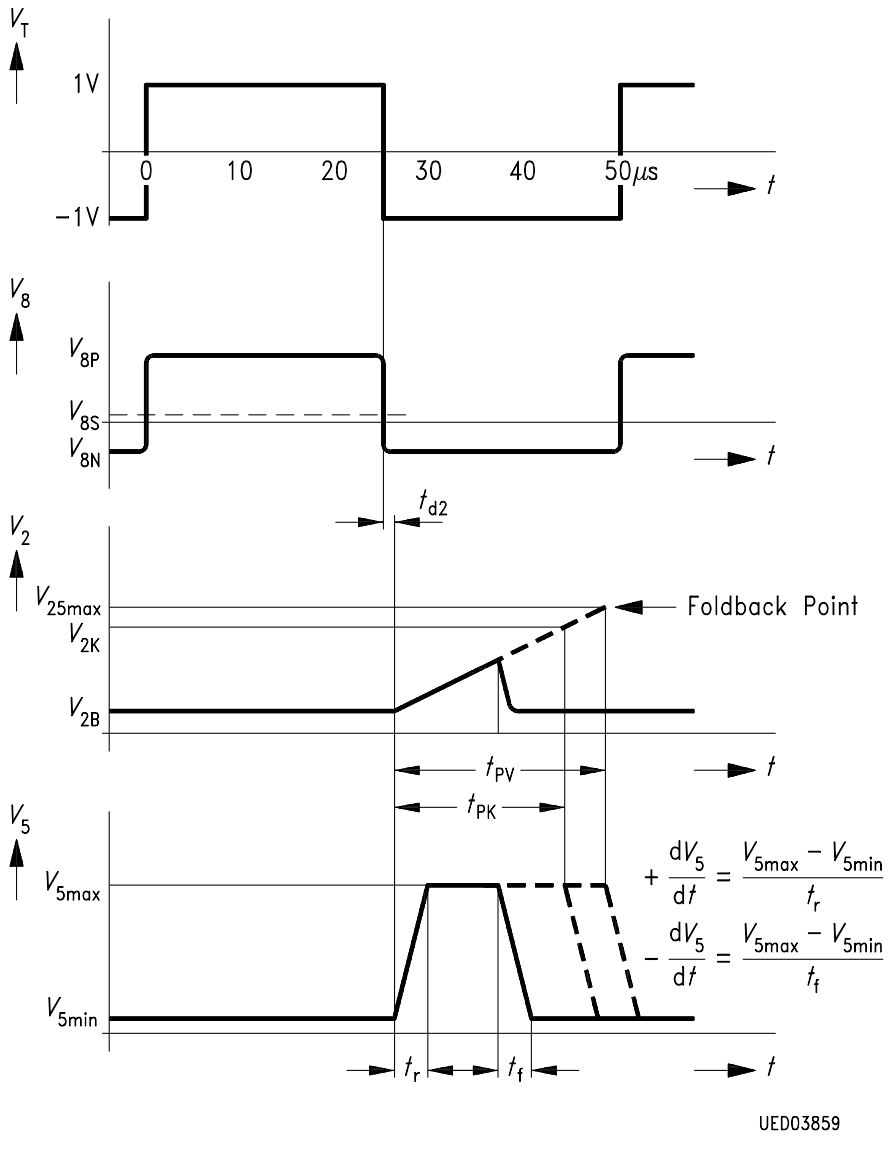
UED00495

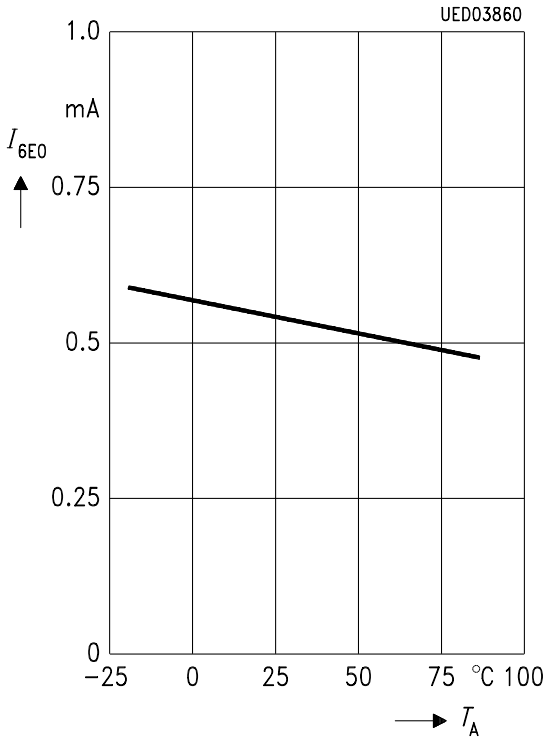


Start-Up Hysteresis

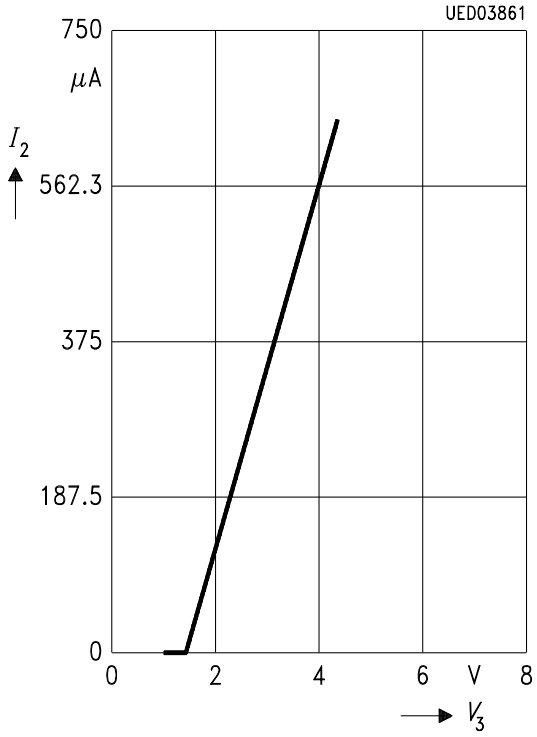


Operation in Test Circuit 2

Start-Up Current as a Function of the Ambient Temperature

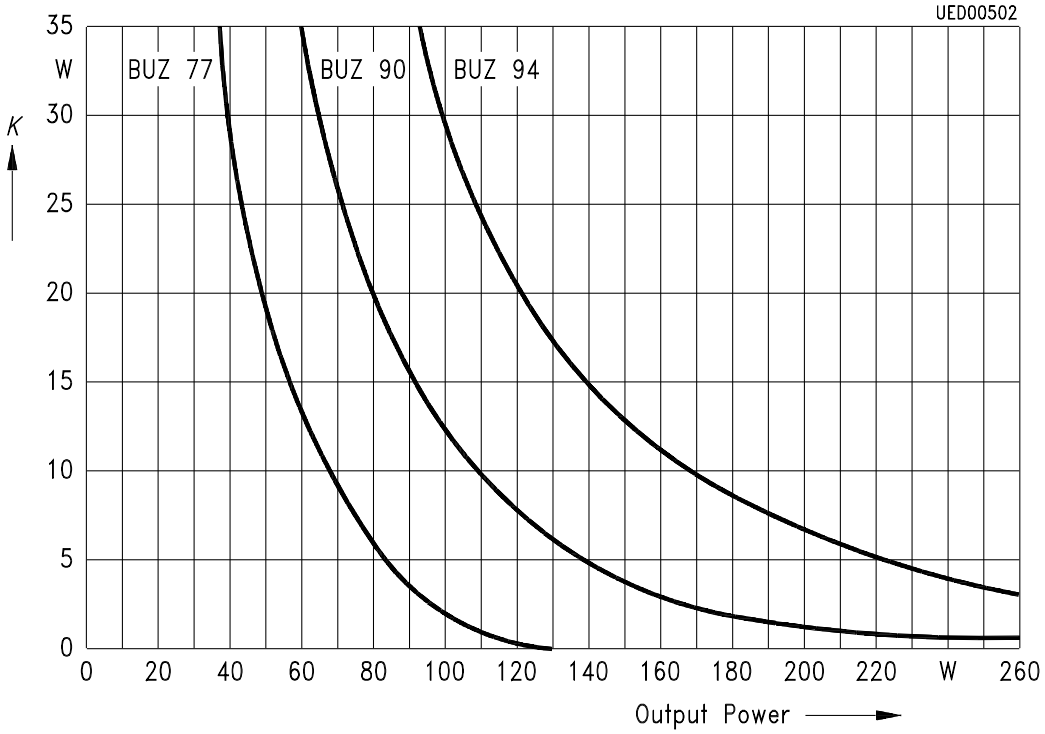


Overload Point Correction as a Function of the Voltage at Pin 3



Recommended Heat Sink by 60 °C Ambient Temperature

Narrow Range 180 V ... 120 V ~



Narrow Range 90 V ... 270 V ~